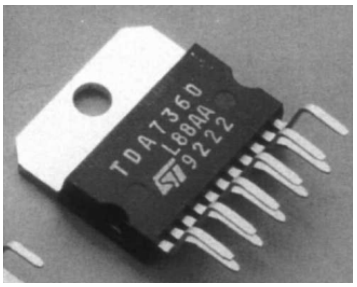
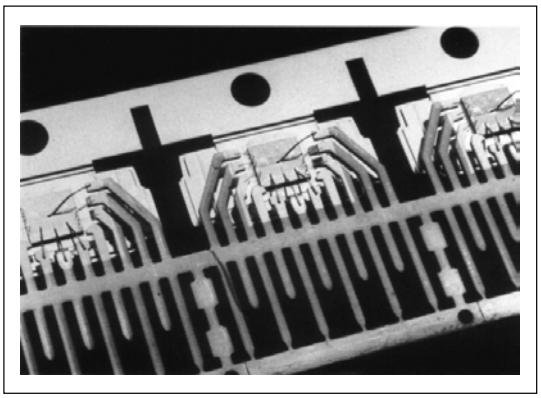
A VLSI Primer

- **VLSI** (Very Large Scale Integration) chips is basically a complex **IC** (Integrated Circuit) chip (**silicon die**) that is placed inside a package (plastic or ceramic) where electrical connection can be made via gold wires attached to a lead frame.
- VLSI chips come in different shapes and sizes, depending on functionality and applications.

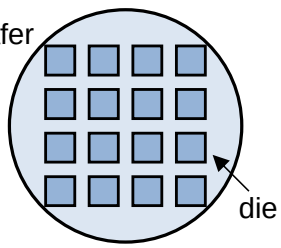




VLSI for Mass Production

- VLSI fabrication technology is based on **photolithography** reproduction techniques —very similar to a printing process for mass production.
- The substrate used for “printing” is the silicon **wafer**.
- The “printing” process consist of a series of processing steps that is used to etch a micro-pattern and/or alter the electrical characteristics of the wafer.
- Cost of the VLSI chip is directly related to die size and processing cost.

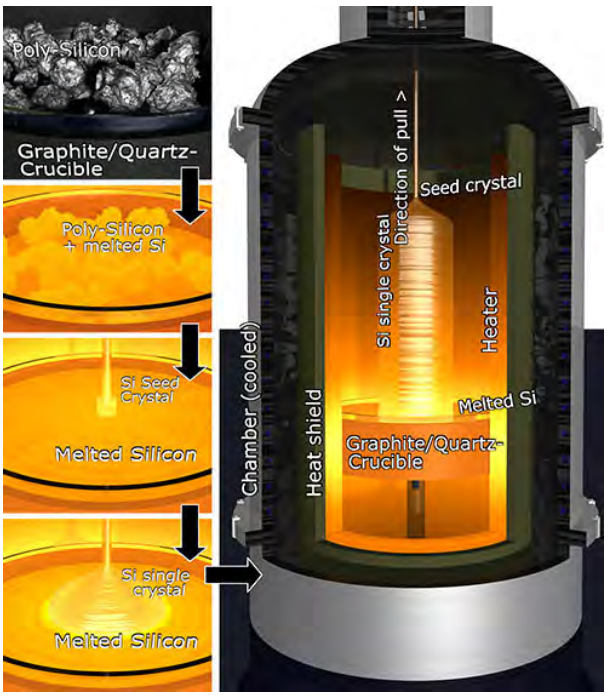
$$\text{Die Cost} = \frac{\text{Die Size}}{\text{Wafer Size}} \times \text{Processing Cost}$$



- Small die size is extremely important.

Starting Material

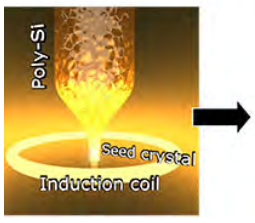
- Electronic-grade polysilicon nuggets are melted in a quartz crucible at a T > 1400°C in an inert gas atmosphere (e.g., argon).
- **Czochralski**-technique (CZ) is a method to pull a monocrystal **ingot** with the same crystallographic orientation of a small monocrystalline seed crystal out of molten silicon



https://www.microchemicals.com/products/wafers/silicon_ingot_production.html

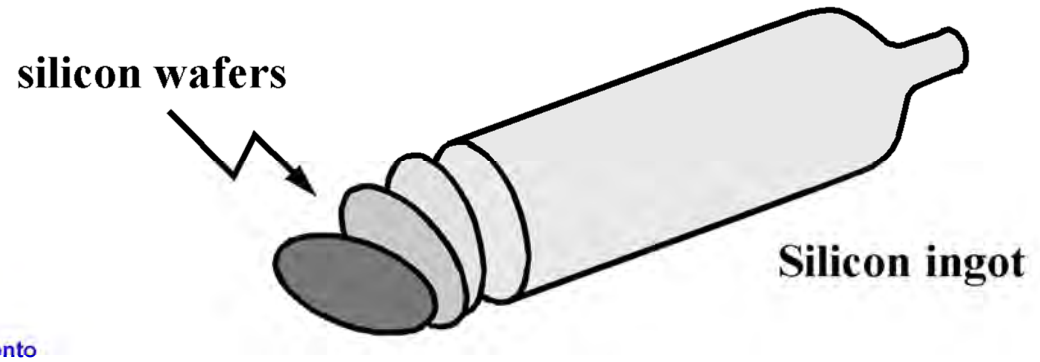
Starting Material (cont'd)

- **Float-Zone** technique is used to re-fine/purify the silicon ingot
- An RF coil melts a small region of the polysilicon which, after cooling down, forms monocrystalline silicon with the crystallographic orientation of the seed crystal (e. g. <100>, <110> or <111>)
- The melted zone move along the entire ingot
- Since most impurities are less soluble in the crystal, the molten zone carries the impurities away to either end of the ingot



Wafer Preparation

- The starting material for modern integrated circuits is very high purity **silicon**. The material is grown as a single crystal **ingot**.
- It takes the shape of a steel gray solid cylinder 10 to 30 cm in diameter and about one meter length.
- This crystal is then sawed (like a loaf of bread) to produce wafers 10 to 30 cm in diameter and 400 to 600μm thick.

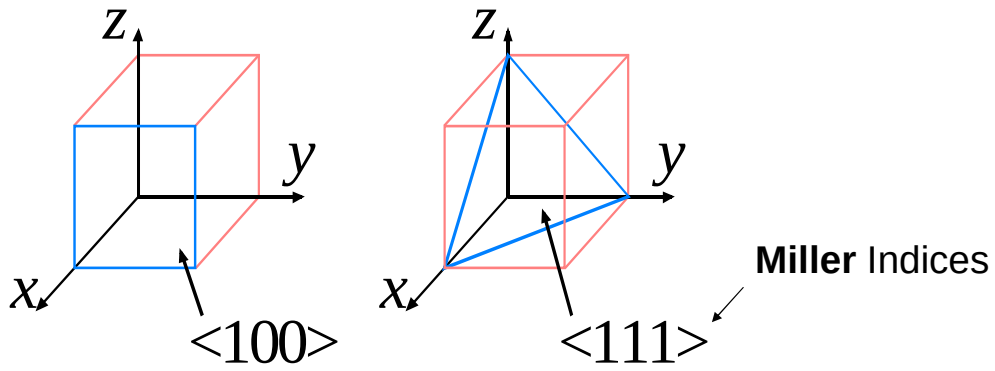


Wafer Preparation (cont'd)

- The sawed wafer surface must be both flat and smooth. This done by a two-steps polishing.
- Rough polishing using a conventional abrasive, slurry-lapping process. This is to remove the surface damage leftover from the wafer-slicing process.
- The wafer is polished to a mirror like finish using chemical and mechanical polishing techniques — a combination of chemical etching and mechanical buffing.
- The wafers are mounted on rotating holders and lowered onto a pad surface rotating in opposite direction. A slurry of silica suspended in a mild **etchant** (e.g., KOH – potassium hydroxide) is used during polishing.

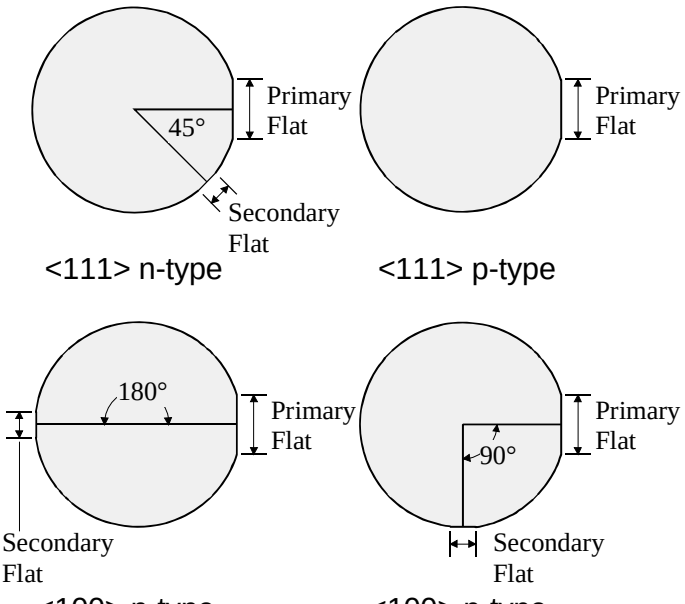
Wafer Preparation (cont'd)

- Semiconductor manufacturers usually purchase ready-made silicon wafers and rarely start their process in ingot form.
- The basic electrical and mechanical properties of the wafer depend on the **orientation** of the crystal growth, the **concentration** and the type of **impurities**.



Wafer Preparation (cont'd)

- The crystal orientation of the wafer is identified by means of primary and secondary flats.



Wafer Preparation (cont'd)

- <100> wafers are usually used for **MOS** ICs.
- <111> wafers are usually used for **bipolar** ICs.
- The crystal orientation can be determined by etching, x-ray diffraction, or light reflection.

Typical 200 mm Wafer Specification	
Diameter	200mm
Diam. Tolerance	0.25mm
Thickness	725 ±50µm
Crystal Orientation	<100> ± 1°
Resistivity	2.7-4 Ωcm
Oxygen	25-29 ppm
Oxygen Gradient	5%
Carbon	0.3 ppm

- Popular wafer sizes in current technology is in 200 and 300mm.

Basic Processing Steps

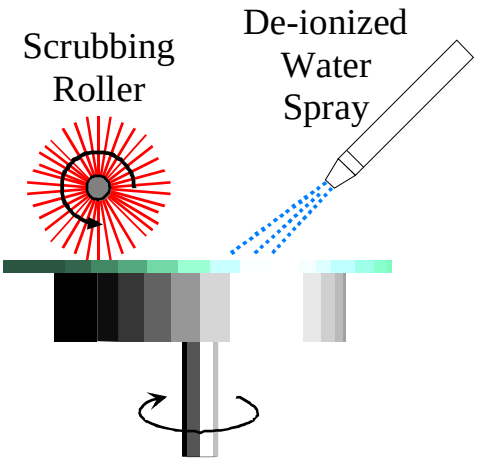
Cleaning

- Clean wafers (free of contaminants) are essential at all stages of the fabrication process, especially before any high temperature operation.
- Cleaning procedures are needed prior to **any** processing steps, consequently wafers spend most of their time in the cleaning station.
- Contaminants in the wafer surface could include:
  - Particulates
  - Organic residues
  - Inorganic residues
  - Unwanted oxide layers

Cleaning (cont'd)

Particulate Removal:

- Blow off using a spray of high-pressure nitrogen.
- Wafer scrubbers: rotating brush and spray of de-ionized water (+ detergent if necessary).
  - Scrubbers are usually stand-alone units with automated loading and cleaning setup.
  - High pressure water cleaning using a small stream of water at 2000 to 4000 psi.
  - A stream of water is used to dislodge both surface particles.



Cleaning (cont'd)

Organic Residue Removal:

- Contaminants that contain carbon, e.g., oil from fingerprints.
- Can be removed using solvent baths such as alcohol or acetone.

Inorganic Residue Removal:

- Contaminants that do not contain carbon.
- A variety of solution can be used:
  Ammonia
  Sulfuric acid,
  Sulfuric acid +
  Hydrogen Peroxide

RCA Clean

- Developed in the mid 60's by RCA engineers.
- 2 steps process to remove organic and inorganic residues.

RCA Clean Type	Parts by Volume
Standard Clean (SC-1)	5: DI water 1: 30% Hydrogen perxoide 1: 29% Amonium hydroxide
Process	70°C for 5 minutes
Standard Clean (SC-2)	6: DI water 1: 30% Hydrogen perxoide 1: 37% Hydrochloric acid
Process	70°C for 5-10 minutes

RCA Clean (cont'd)

Oxide Removal:

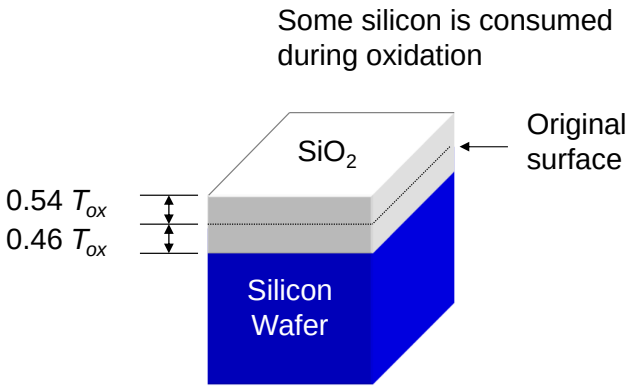
- Silicon can be oxidized very easily, whenever it is exposed to **oxidants**.
- **Oxides** are often grown in the baths. Typically, 100 to 200Å is thick enough to block the silicon surface from reacting properly.
- Silicon surfaces with an oxide are called **hydroscopic**.
- Surfaces without oxide are called **hydrophobic**.
- **Hydrofluoric** (HF) acid is often used to remove the oxide. HF does not etch silicon.

Rinse and Dry

- Wafers are loaded onto a cassette and go through rinse and dry spinner

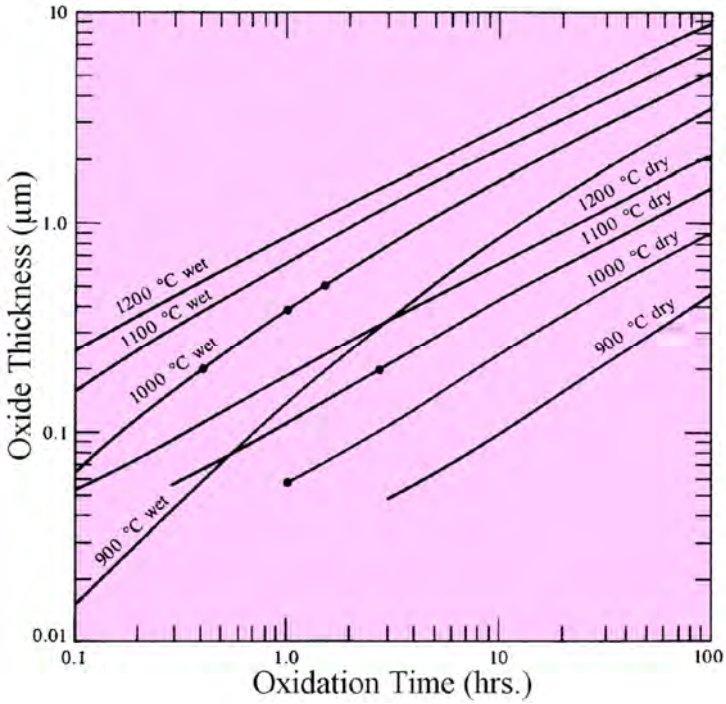
Oxidation

- $Si + O_2 \Rightarrow SiO_2$ **Dry oxidation**
- $Si + 2H_2O \Rightarrow SiO_2 + H_2$ **Wet Oxidation**



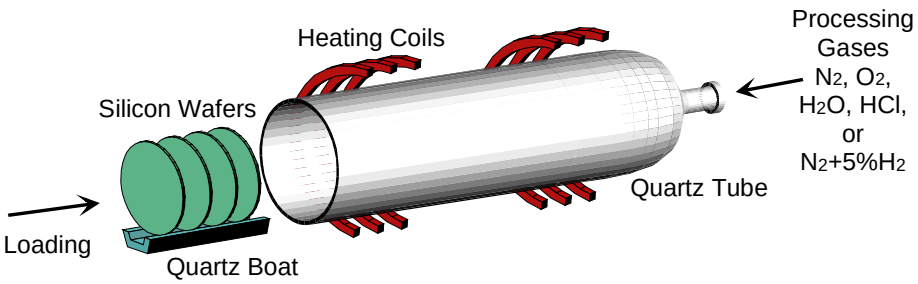
- Thermal oxidation is easily achieved by heating the wafer to a high temperature, typically 900 to 1200°C in pure oxygen or steam environment.
- Oxygen diffuses to the silicon surface, reacts and forms SiO_2.

Oxidation rate for <100> silicon



Oxidation (cont'd)

- Thermal oxidation is carried out in a high temperature furnace tube.
- The tubes are usually made of **quartz** or **silicon carbide**.



Furnace Model:	Bruce Systems Diffusion Furnace
Heating Method:	Resistive, Microprocessor Controlled
Temperature Range:	200 °C to 1150 °C
Ramp Rate:	approx. 10 °C/min
Wafer Size:	3" and 4"

Oxidation (cont'd)

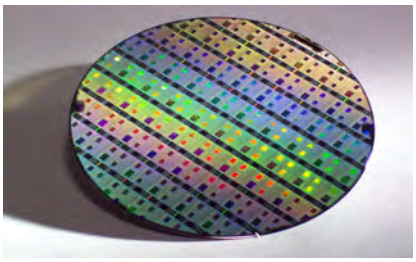
- Oxide Quality: thickness uniformity, breakdown voltage, trapped charges.
- Thin oxide is usually grown using dry oxidation
  Thick oxide is usually grown using wet oxidation
- Dry oxidation results in slower growth rate, but high density — higher breakdown voltage.
- MOS devices are usually fabricated using <100> wafers since the SiO_2-Si interface has the lowest number of dangling bonds.
- **Sodium** contamination results in positive mobile charges which could lead to a shift in the threshold voltage of the MOS devices.

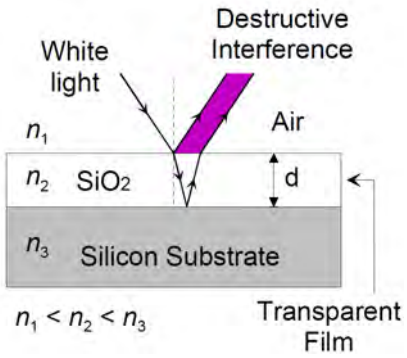
Oxidation and Diffusion Furnaces

- The furnaces normally have multi-stack of tubes
- Each tube is dedicated to one function only, e.g. oxidation, diffusion

- Motorized loading tray pushes the wafer boat slowly into the red-hot furnace
- This temperature ramp up and ramp down time (~ 30 min) is very critical

Characterization of Oxide Films



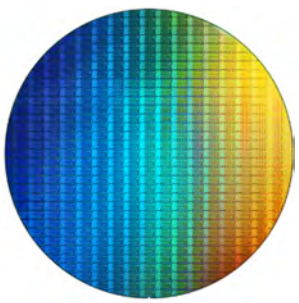


Film Thickness (Å)	Color of Film (those shown are only indicative)
500	tan
700	brown
1000	dark violet to red violet
1200	royal blue
1500	light blue to metallic blue
1700	metallic to very light yellow-green
2000	light gold or yellow - slightly metallic
2200	gold with slight yellow-orange
2500	orange to melon
2700	red-violet
3000	blue to violet-blue
3100	blue
3200	blue to blue-green
3400	light green
3500	green to yellow-green
3600	yellow-green
3700	green-yellow
3900	yellow
4100	light orange
4200	carnation pink
4400	violet-red
4600	red-violet
4700	violet
4800	blue-violet
4900	blue
5000	blue-green
5200	green

source: ECE Illinois - ece444: GT7 - Oxide Thickness Color Chart

Uniformity of Oxide Thickness

- The thickness of the SiO_2 can determine various electrical parameters such as threshold voltage, V_{TH}, breakdown voltage, *BV*, etc.
- A visual inspection of the color pattern on the wafer can be a quick indication of the uniformity

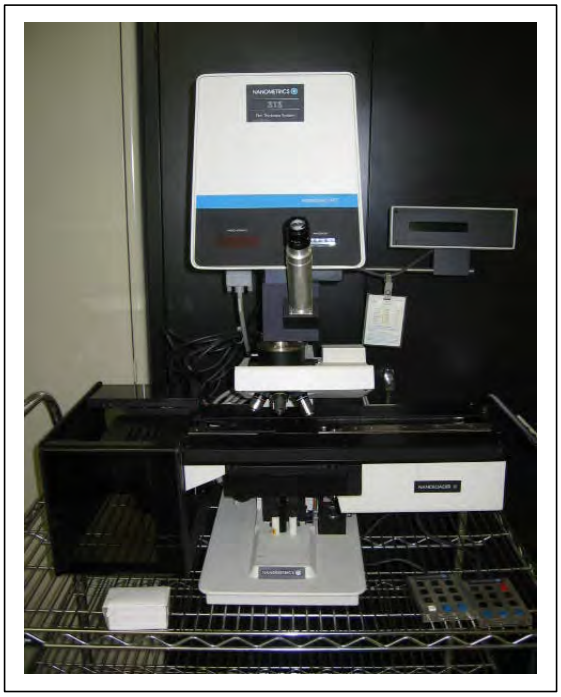


Characterization of Oxide Films

- There are many different methods to measure the oxide thickness
  - Light diffraction → Nanospec AFT

    This uses reflectometry (measurement of reflected light) to determine film thicknesses based on interference effects

    Using measurement algorithms, the Nanospec compares a bare silicon wafer to the sample being tested to yield thickness information without causing damage to the sample



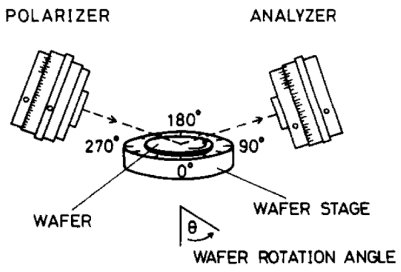
Characterization of Oxide Films

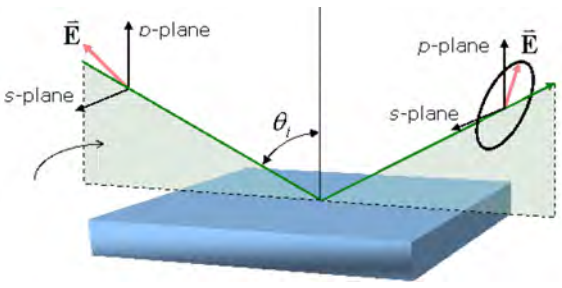
- There are many different methods to measure the oxide thickness
  - Ellipsometry:

    Three types of data are typically acquired with the ellipsometer, transmission and reflection intensity and ellipsometry

    Ellipsometry measures the change in polarization state of light reflected from the surface of a sample

    highly accurate and reproducible





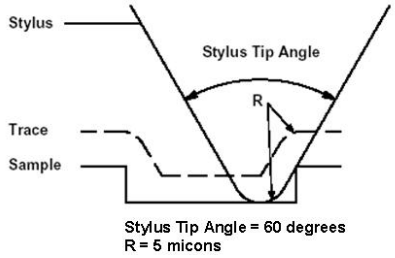
Source:
http://www.uta.edu/optics/research/ellipsometry/ellipsometry.htm

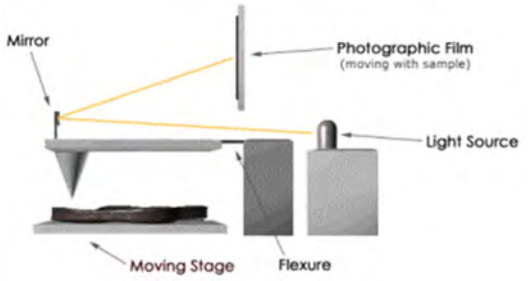
Characterization of Oxide Films

- There are many different methods to measure the oxide thickness
  - Surface Profiler → Tencor Alpha-Step

    a mechanical, stylus-based step profiler that can measure step heights up to 2 millimeters

    a dedicated wafer sample is required



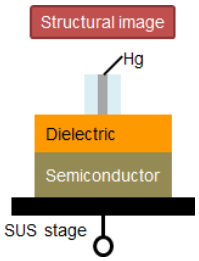


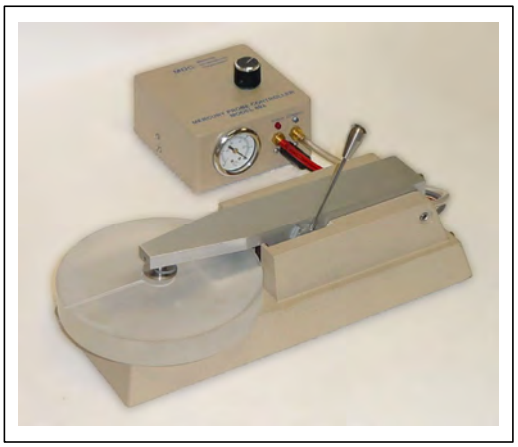
Source: http://microlab.berkeley.edu/labmanual/chap8/asiq.pdf

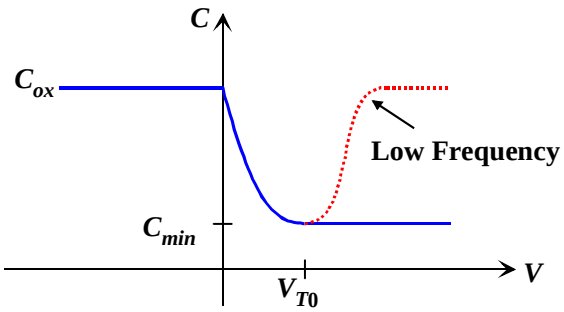
Characterization of Oxide Films

- There are many different methods to measure the oxide thickness
  - CV measurement

    a mercury probing station is used to forma MOS capacitor on a bare silicon wafer with an oxide film







$$C = \frac{C_{ox}C_d}{C_{ox} + C_d}$$

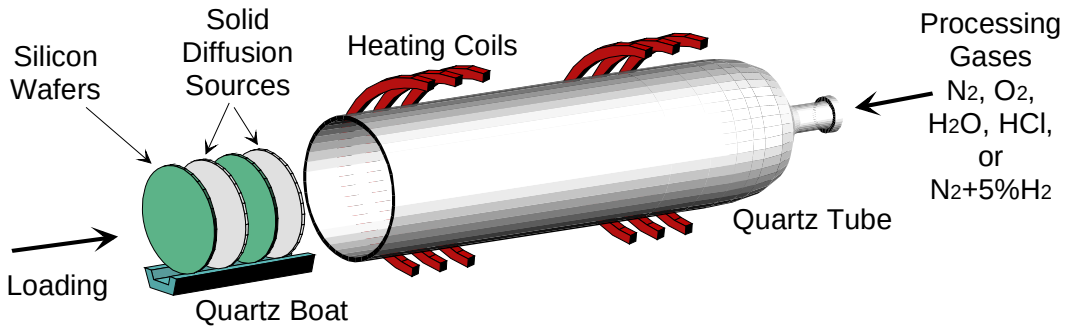
Source: http://microlab.berkeley.edu/labmanual/chap8/asiq.pdf

Diffusion

- **Diffusion** is the process by which atoms move through the crystal lattice. This is very much like a drop of ink disperse through a glass of water except that it occurs very slowly in solids.
- The impurity atoms (**dopants**) changes the resistivity of the silicon.
- The rate at which dopants diffuse in silicon is a strong function of temperature.
- Diffusion of impurities is usually carried out at high temperatures (1000 to 1200°C) to obtain the desired **doping profile**.

Diffusion (cont'd)

- When the wafer is cooled to room temperature, the impurities are essentially "frozen" in position.
- The diffusion process is performed in furnaces similar to those used for oxidation. The depth to which the impurities diffuse depends on both the temperature and time.

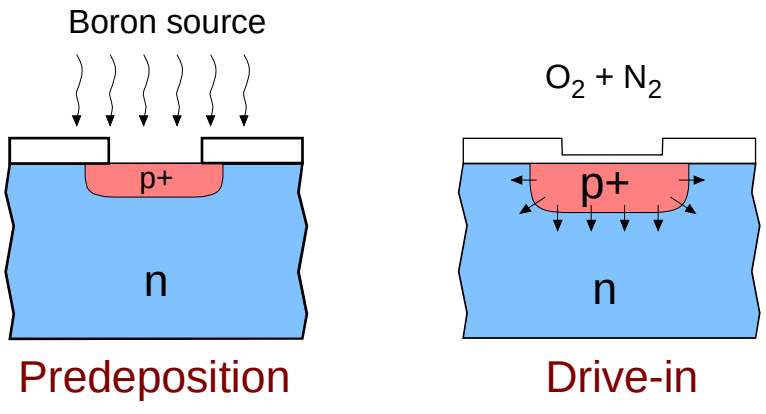


Diffusion (cont'd)

- The most common impurities used as dopants are **boron**, **phosphorus** and **arsenic**. Boron is a **p-type** dopant while phosphorus and arsenic are **n-type** dopant.
- These dopants can be effectively masked by thin silicon dioxide layers.
- Diffusion is usually carried out in two steps: **pre-deposition** and **drive-in**.

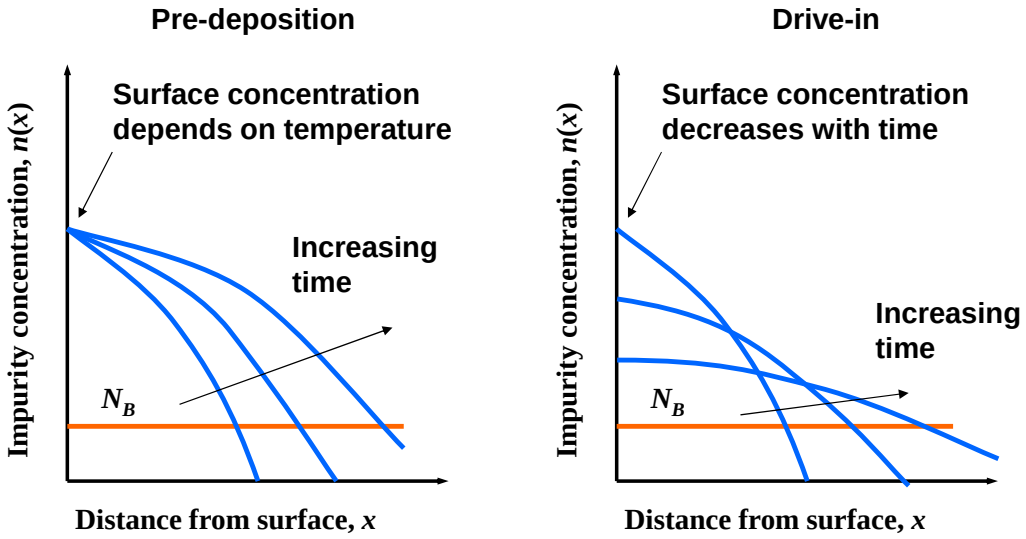
Diffusion (cont'd)

- Pre-deposition is a **constant source diffusion** where a continuous flow of impurity is dissolved into the wafer surface.
- Drive-in is used to move the diffusion front to the desired depth (junction depth).



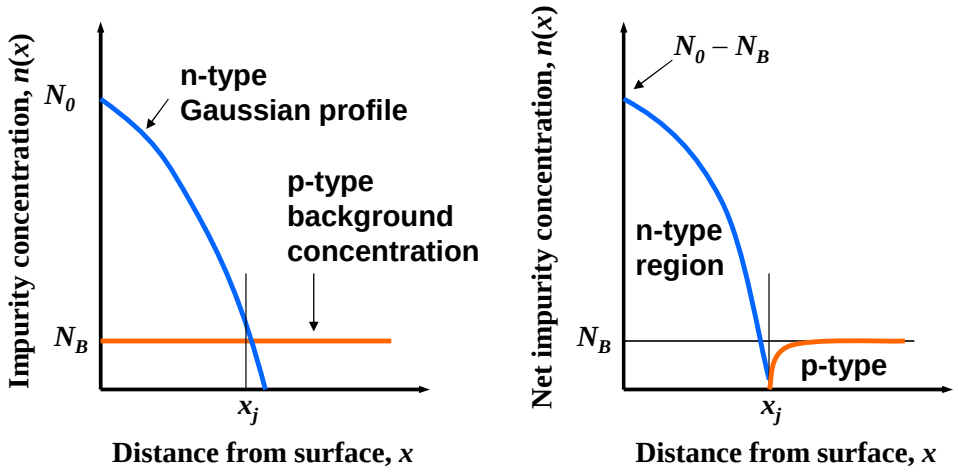
Diffusion (cont'd)

- During this step, the source of impurity is removed. The only amount of impurity available is from the pre-deposition step.



Diffusion (cont'd)

- The goal of most diffusion is to form ***pn*** junctions by converting p-type material to n-type or vice versa.
- The point at which the impurity profiles intersects is the **metallurgical junction depth**, x_j.

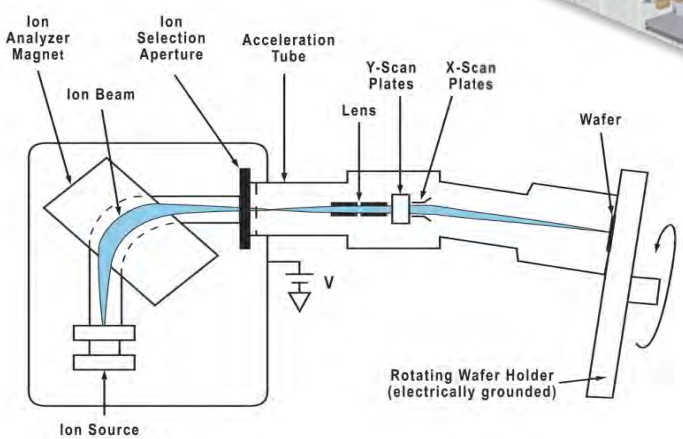


Ion Implantation

- **Ion implantation** is an alternate method used to introduce impurities into silicon.
- An ion implanter produces ions of the desired impurity, accelerates them by an electric field, and allows them to strike the silicon surface.
- The ions become embedded in the silicon. The depth of penetration is related to the energy of the ion beam, which can be controlled by the accelerating-field voltage (energy specified in keV).
- The **dose** of ions implanted (specified in cm^{-2}) can be controlled by varying the beam current.

Ion Implantation

- **Ion implantation** is carried out using a machine that uses magnetic field to separate the desired ions from other impurities
- An electric field is used to accelerate the ions towards the wafer



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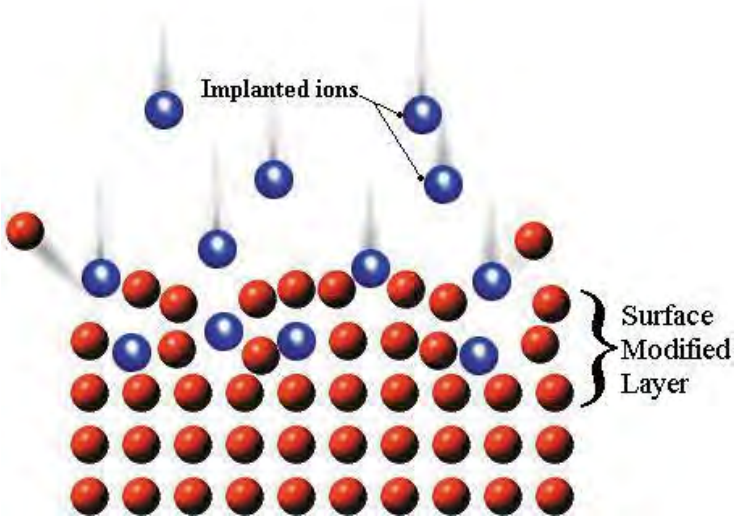
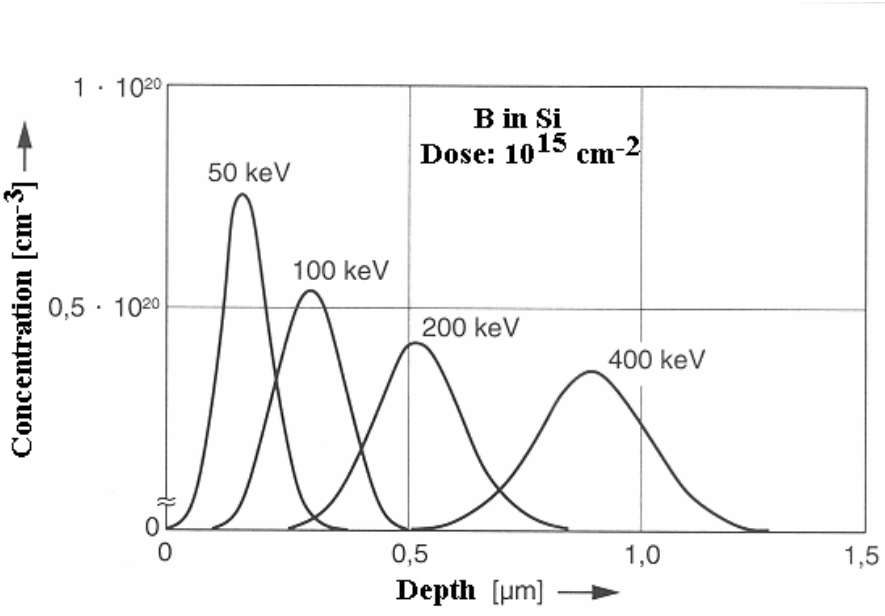
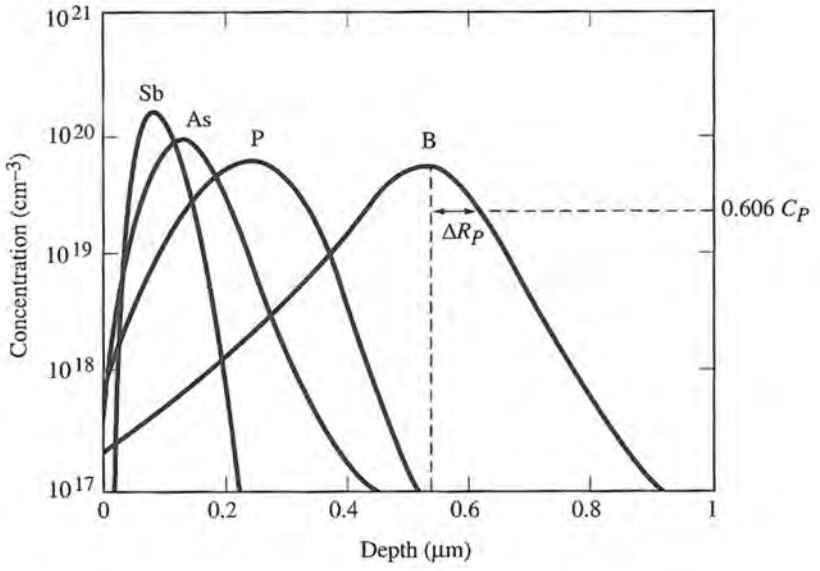


Implantation Depth Controlled by Ion Energy



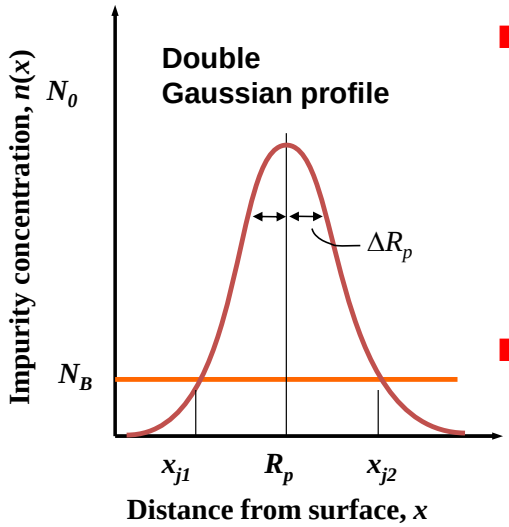
Implantation Depth Varies with Dopant

- Larger, heavier particles do not penetrate as deeply



Ion Implantation (cont'd)

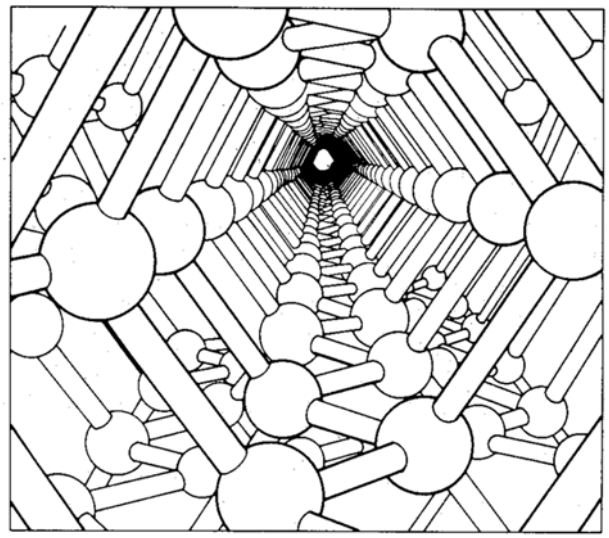
- Since both voltage and current can be accurately measured and controlled, ion implantation results in much more accurate and reproducible impurity profiles than can be obtained by diffusion.



- Ion implantation can be performed at room temperature. Ion implantation normally is used when accurate control of the dopant is essential for device operation.
- The impurity profile is characterized by the **range**, R_p and **straggle**, ΔR_p.

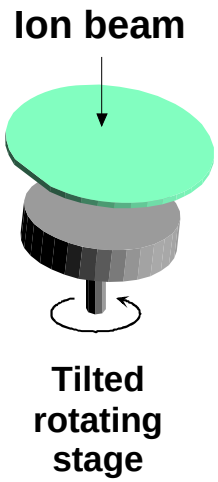
Ion Implantation (cont'd)

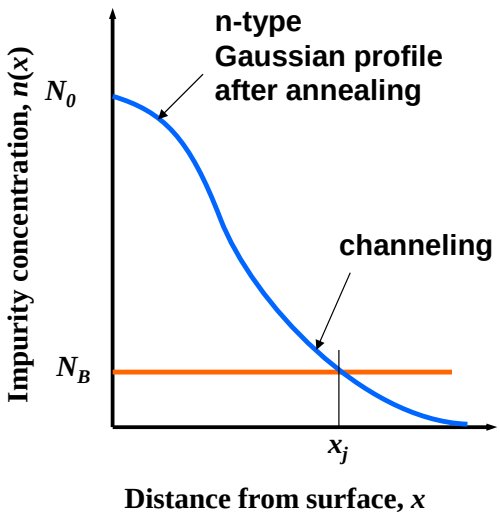
- The impurity must be subjected to a high temperature activation (similar to drive-in, except it is usually for a much shorter time) to reduce crystal lattice damage.
  - The regular arrangement of silicon lattice in <110> orientation leaves a large amount of open space.
  - The implanted ions may channel deep into the substrate.



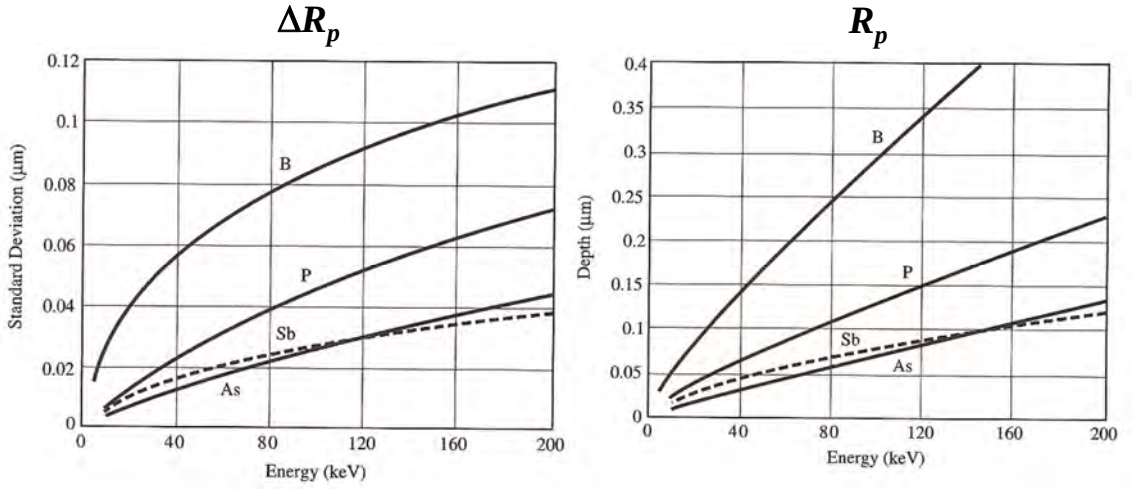
Ion Implantation (cont'd)

- **Channeling** can be reduced by tilting the <100> silicon by approximately 7° relative to the ion beam.
- **Tilted** implant can produce a doping profile with a junction depth that is closer to the theoretical calculation.





Penetration Depth as a Function of Energy

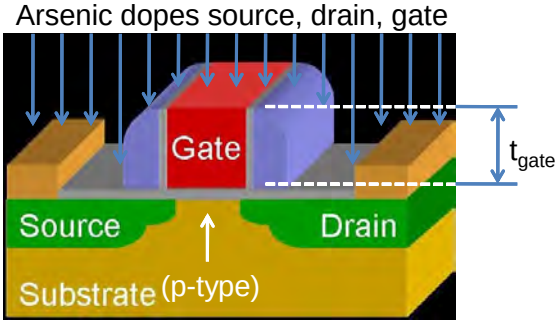


Ion Implantation Example

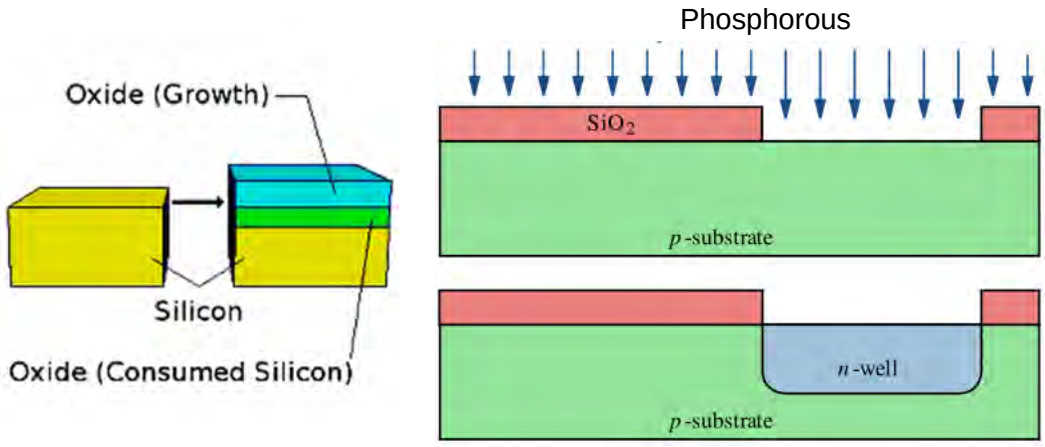
- Dose = number of implanted ions =
- Energy = 50 keV
- N_B = 1x10^{16} cm^{-3}
- Neglect gate oxide thickness.
- Find minimum t_{gate} so that Arsenic does not affect the channel doping.

$$Q = \int_{-\infty}^{\infty} N(x)dx$$
$$= \sqrt{2\pi}\Delta R_P C_P$$
$$= 2\times10^{15} cm^{-2}$$

Arsenic dopes source, drain, gate



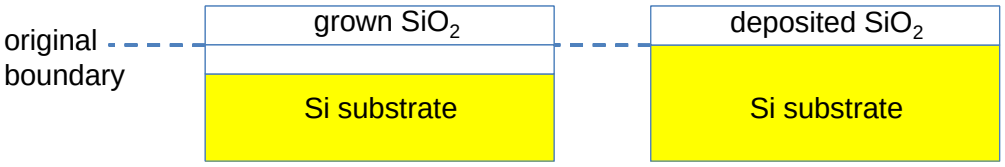
We now know how to modify existing silicon



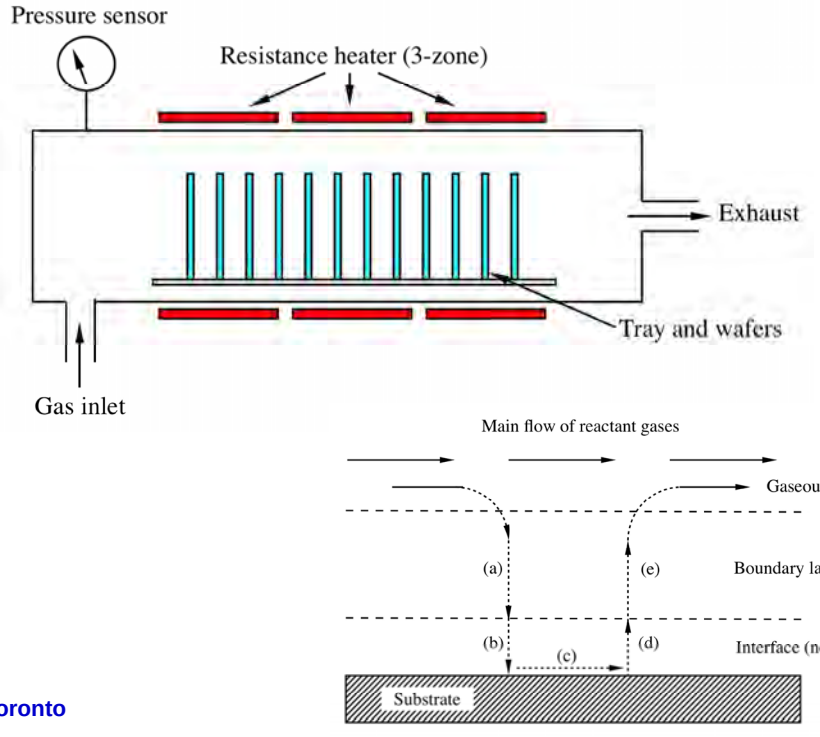
What if we want to ADD to the silicon instead of modifying what is already present?

Chemical Vapor Deposition (CVD)

- A process by which gases or vapors are chemically reacted, leading to the formation of a solid on a substrate.
- Example: deposit SiO_2 on a Si substrate by using **silane** gas (SiH_4) and oxygen.
- The oxide layer formed is not as good as a grown oxide. Advantage is that oxide deposits at a faster rate and a lower temperature (below 500°C).

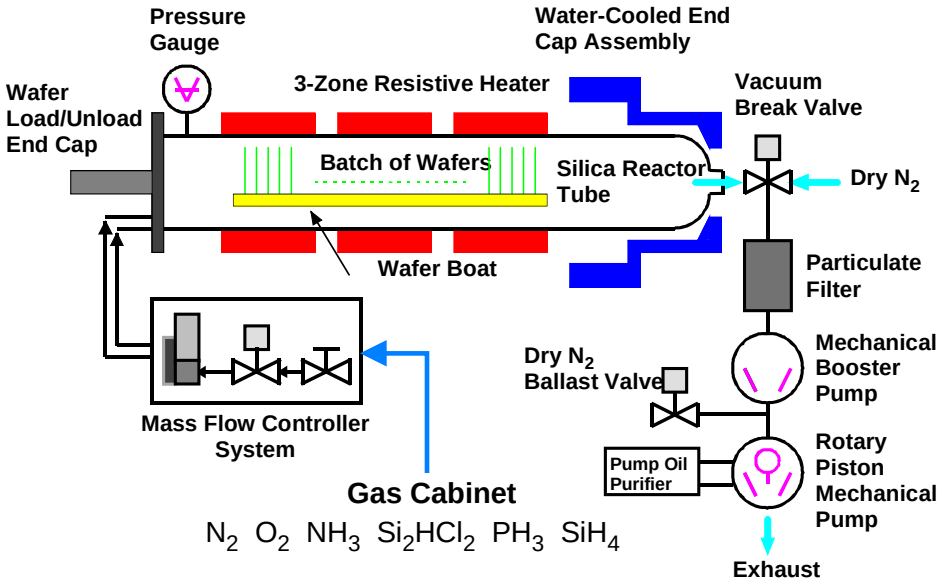


CVD Process



CVD (cont'd)

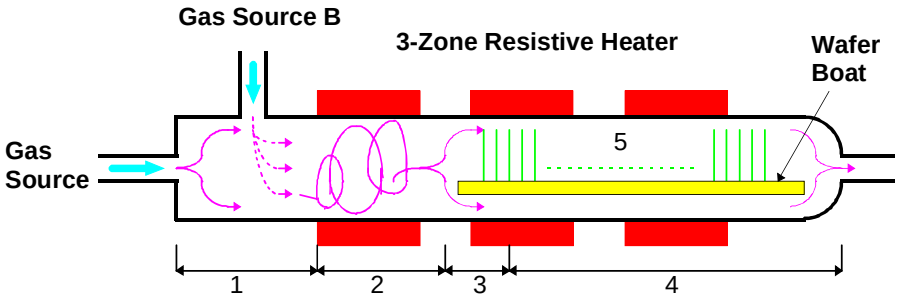
Horizontal LPCVD Reactor



CVD (cont'd)

- If **silane** gas alone is used, a silicon layer deposits on the wafer. The size of the crystalline depends on the deposition temperature.

Transport Phenomena in Horizontal LPCVD Reactor



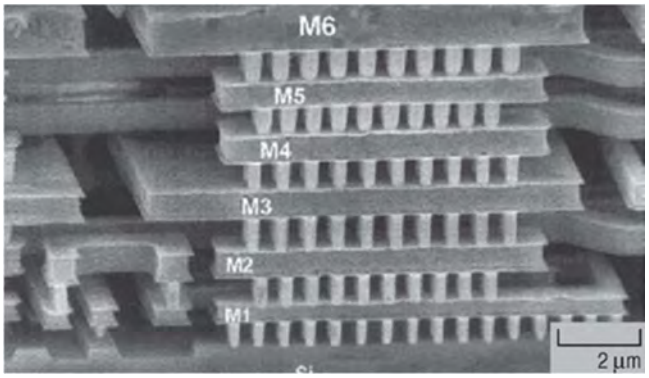
1. **Diffusion Mixing**
2. **Temperature Flow Pattern Developing Zone**
3. **Developing Zone**
4. **Fully Developed Flow Axial Dispersion**
5. **Radial Diffusion Between**

CVD (cont'd)

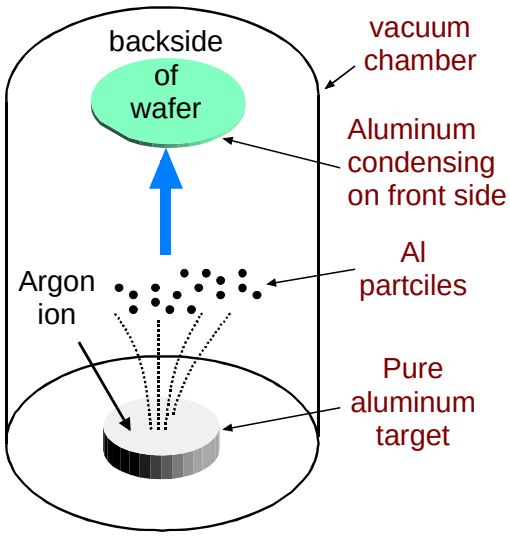
- This is because the atoms have enough energy to align themselves in the proper crystal direction.
- This layer is an **epitaxial layer**, and the deposition process is referred to as **epitaxy** instead of CVD.
- At lower temperatures, or if the substrate surface is not single-crystal Si, the atoms are not all aligned along the same crystal direction. This layer is called **polycrystalline** Si, since it consists of many small crystals of Si aligned in various directions.
- **Polysilicon** layers are normally doped very heavily to form a high conductivity region that can be used for interconnecting devices.

Metallization

- Interconnect the various components of the IC to form the desired circuit.
- Deposition of a metal (aluminum) over the entire surface of the Si, then selectively etched.
- The aluminum is deposited by heating it in vacuum until it vaporizes (melting point of Al = 660^0C).
- The vapors then contact the silicon surface and condense to form a solid aluminum layer.



Sputtering

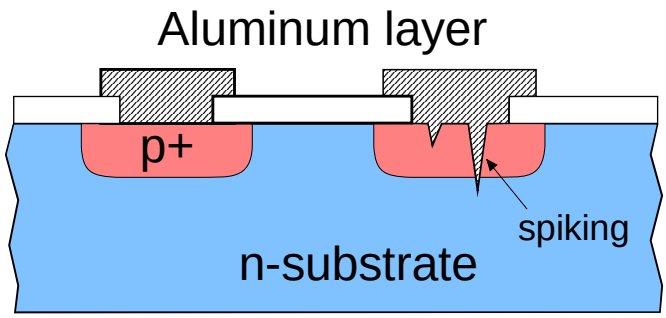


Metallization (cont'd)

- Si melts at 1412°C, Al melts at 660°C. When Si + Al are alloyed together, it exhibits an "**eutectic**" characteristics such that the melting point of 577°C is lower then either of the element alone.
- Because of this low eutectic temperature, metallization is usually performed at the very late stages of the fabrication process.
- After the deposition, the aluminum is usually annealed in an inert atmosphere (e.g. 30 min, 450°C).
- Although this temperature is well below the melting point of aluminum, some silicon may diffuse into the aluminum.

Metallization (cont'd)

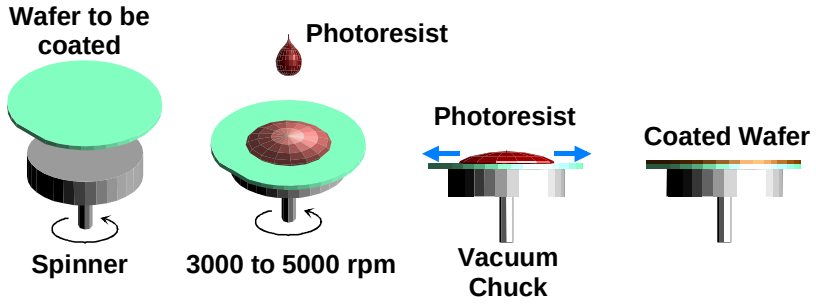
- Anywhere aluminum comes into contact with silicon, some silicon will be absorbed, leaving avoids behind.
- Since this is not a uniform process, random pits may result. After the annealing, aluminum will fill up these voids, resulting in spikes penetrating through the surface.



- Spikes may short circuit shallow junctions.
- Use 1% Al-Si target
- Metal **silicide** barriers Ti-Si, Pt-Si, etc.

Photolithography

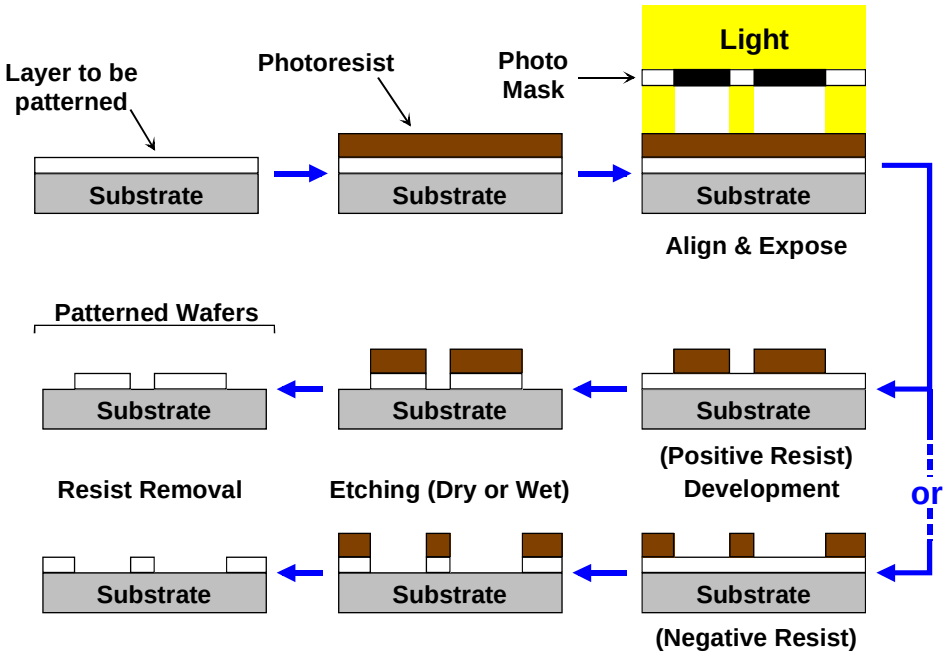
- The surface geometry of the various integrated-circuit components is defined photographically.
- The silicon surface is coated with a photosensitive layer called **photoresist**.
- To achieve uniform thickness, the photoresist is spin coated onto the silicon wafer.



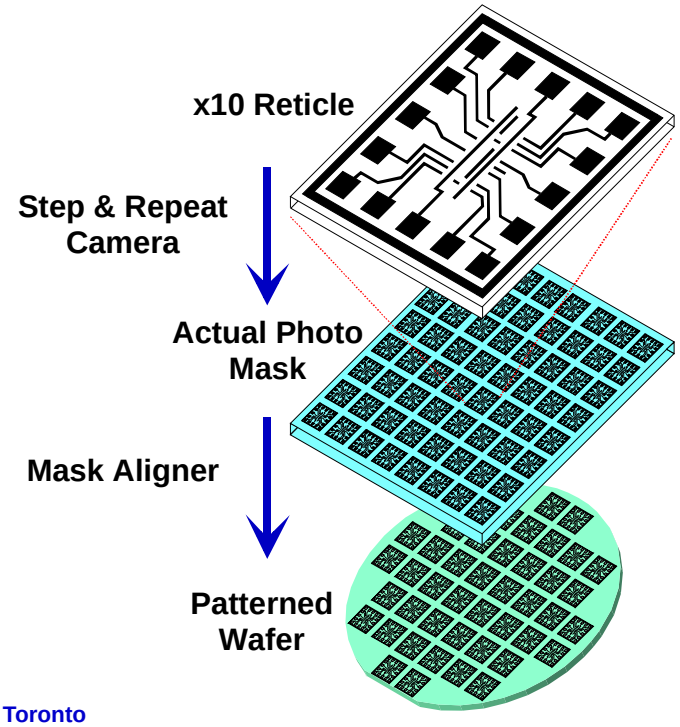
Photolithography (cont'd)

- The photoresist may be softened if exposed to light (**positive resist**) or soften if not exposed (negative).
- The softened layer can then be removed using a chemical developer, causing the mask pattern to appear on the wafer.
- Very fine surface geometries can be reproduced accurately by this technique.
- The photoresist layer forms an effective mask from the chemical etchants used for silicon dioxide or aluminum.
- This allows "windows" to be etched in the oxide layer in preparation for subsequent diffusion processes.

Wafer patterning



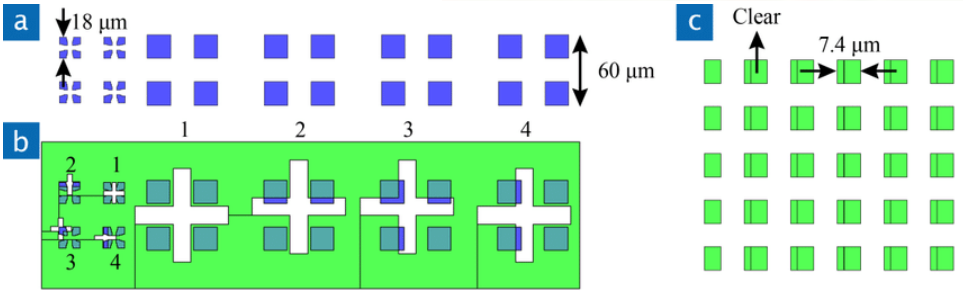
Photolithography



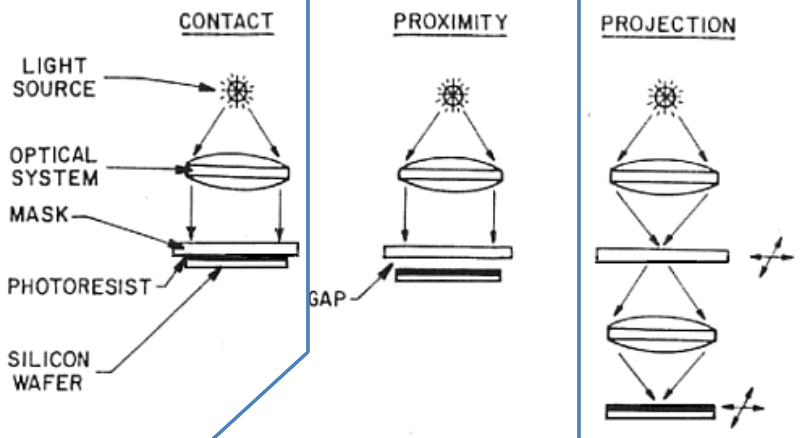
- The x10 mask is generated from computer layout.
- A step and repeat camera is used to generate an array of dies on the final mask.
- The final mask is then used in the actual patterning.
- Multiple masks must be aligned on top of each other.

Photolithography (cont'd)

- A mask aligner is used to expose the mask pattern on the proper location with respect to the existing patterns on the silicon wafer
- Special alignment marks allow vision recognition and automatic adjustment



Wafer Exposure Systems



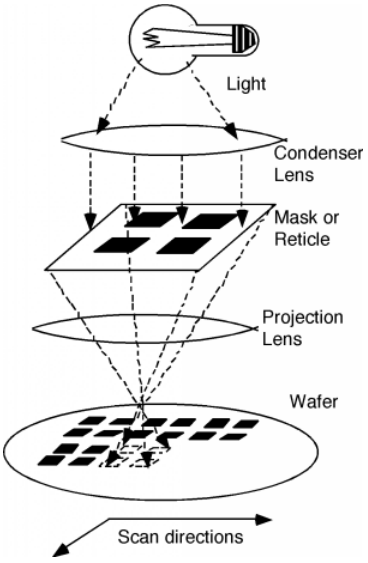
Minimized diffraction.
Physical contact can damage mask and photoresist layer.

Low number of defects.
Gap creates diffraction – small features not possible.

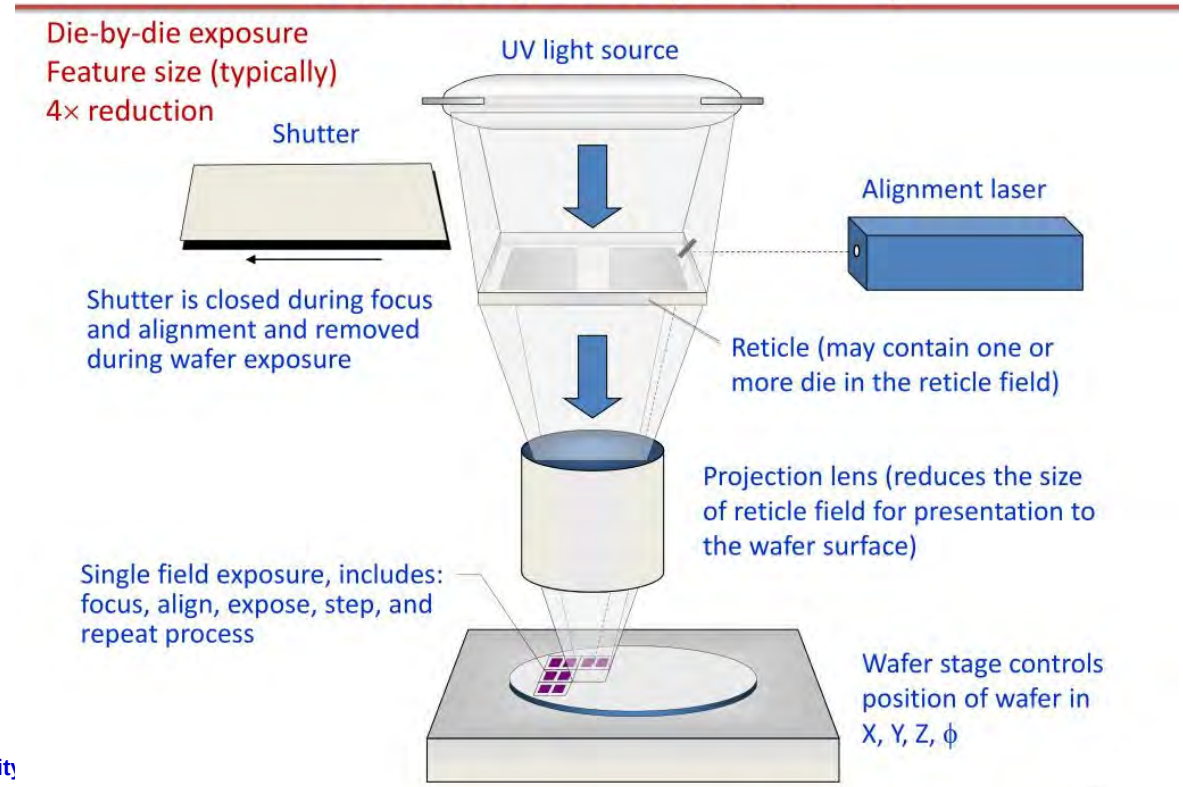
Low number of defects.
High resolution.

Projection Printing

- The x10 mask is generated from computer layout.
- A step and repeat camera is used to generate an array of dies on the final mask.
- Multiple masks must be aligned on top of each other.
- Modern machines capable of printing on 50 wafers per hour.

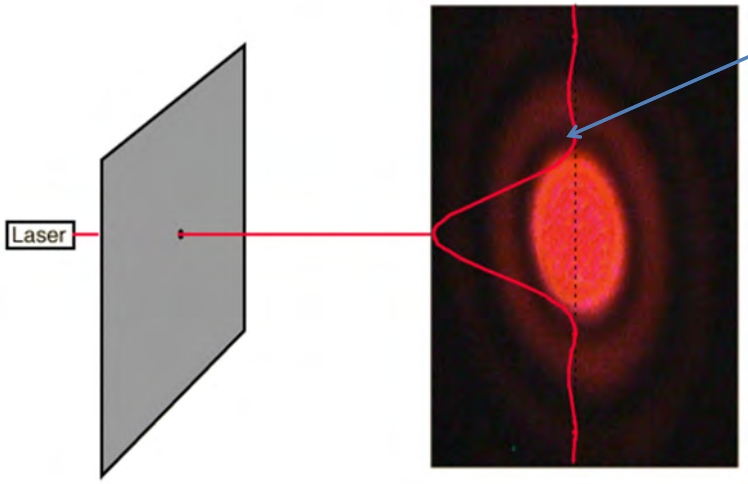


Stepper (step and repeat system)



https://www.slideserve.com/shalin/introduction-and-application-light-source-and-photomask-alignment-photolithography-systems-resolution-depth-of-focus-modulation-transfer-function

Diffraction



Radius of central max =

$$\frac{1.22\lambda f}{d}$$

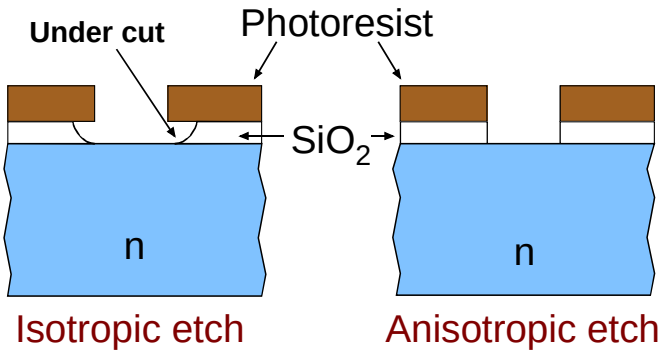
d = focusing lens diameter
f = focal length
λ = **wavelength**

Etching

- Chemical etching in liquid or gaseous form is used to remove any barrier material not protected by hardened photoresist.
- The choice of chemicals depend on the material to be etched (e.g. SiO2, nitride, poly, metal, etc.).
- **Wet Etch** uses liquid chemical:
  - **Buffered Hydroflouric** Acid (BHF) for SiO_2
  - **Potassium Hydroxide** (KOH) for Silicon
  - **Phosphroic Acid** for Aluminum
  - Hot Phosphroic Acid (180°C) for **Silicon Nitride**

Etching (cont'd)

- **Wet Etch** is usually non-direction. This phenomenon is called **isotropic** etching.
- In the idea case, vertical sidewalls are expected. This type of etching is called **anisotropic** etching
- The etch time and temperature are critical such that over-etch can be avoided.



Etching (cont'd)

- **Wet Etch** has various limitations for small geomerties:
  - limited to pattern sizes of 3μm or larger
  - Isotropic, resulting in sloped sidewalls
  - Requires rinse and dry steps
  - wet chemicals are hazardous and/or toxic
  - potential for contamination
  - failure of resist-wafer bond causes undercutting
- **Dry Etch** processes are more suitable for small feature sizes.

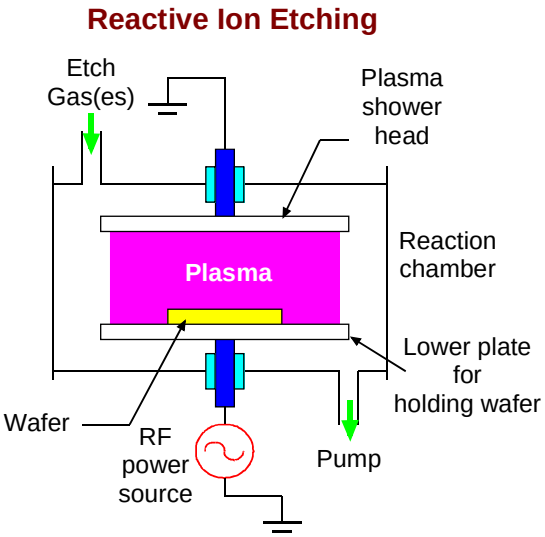
Etching (cont'd)

- Dry Etch is a generic term that refers to the etching techniques in which gases are the primary etch medium.
- The wafers are etched without wet chemicals or rinsing.
- The wafers enter and leave the etching system in dry state.
- There are three dry etching techniques: **plasma**, **ion-milling**, and **reactive ion etching** (RIE).
- Plasma etching uses corrosive gases and plasma energy to cause the chemical reaction.

Etching (cont'd)

- **Ion-milling** uses ion-beam (inert gas, Ar) to physically bombard the wafer surface.
- Small amount of wafer material is literally blasted out of the surface.
- The material removal is highly directional, resulting in good definition of small openings.
- Being a physical process, ion-milling has very poor selectivity, and may be prone to radiation damage.
- **Reactive Ion Etching** (RIE) is a combination of plasma etching and ion-milling principles.

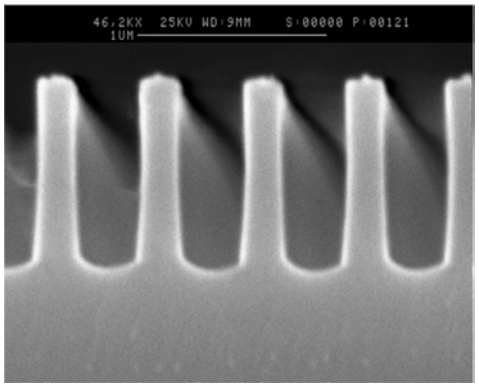
Etching (cont'd)



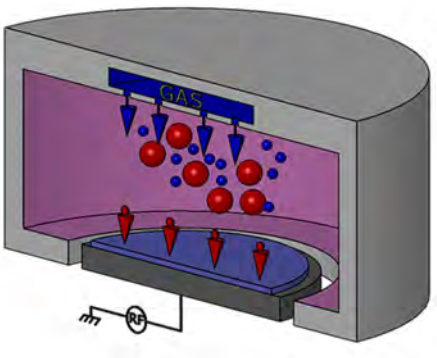
- RIE combines the benefits of chemical plasma etching along with that of directional ion milling.
- The combination etch results in a **selectivity** ratio between SiO_2 and Si in excess of 35:1 compare to 10:1 in plasma only etching.
- RIE has become the choice for all advanced processes.

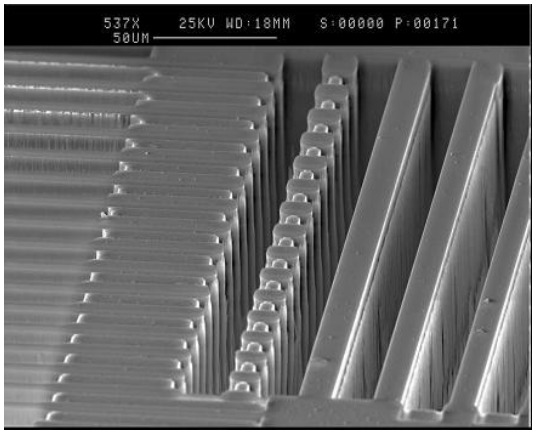
Etching (cont'd)

- Many interesting structures with very fine geometries can be achieved with RIE



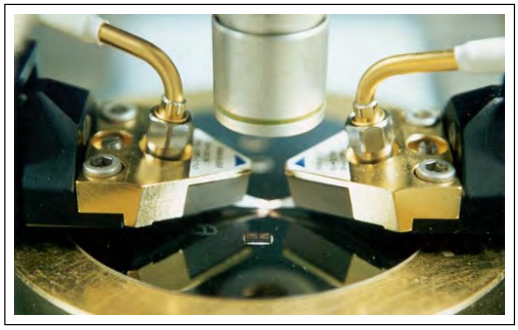
Vertical SiO_2 trenches

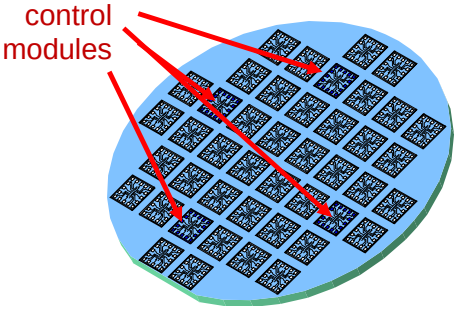




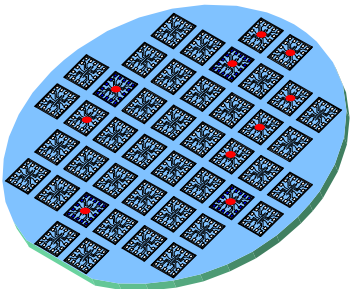
Wafer Probing

- For quick on-wafer testing, the probing station with an adjustable array of fine needle probes is used.
- Special process control modules on the wafer are used for parametric testing.





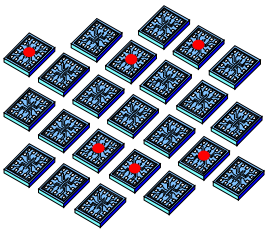
Wafer Probing (cont'd)



- Later, when the dice are separated, any die marked with an ink spot is discarded.
- Complete functional testing is usually too time consuming and often impossible. Instead a minimum sequence of tests is used to determine functionality to an acceptable confidence level.
- Wafer probing is usually limited to DC or simple testing. Full speed or high frequency performance cannot be performed due to load effect of the large parasitic capacitance.

Identification and Separation

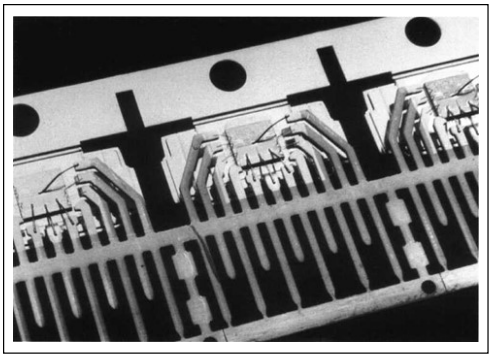
- Following testing, individual dice must be separated.
- The wafer is either scribed using a diamond tip scriber or cut by a circular saw.



- In <100> natural cleavage planes exist perpendicular to the surface of the wafer in directions both perpendicular and parallel to the wafer flats.
- Following scribing, the wafer is place upside down on a soft support. A roller applies pressure to the wafer and causes fracture along the scribe lines.

Die attachment and Wire Bonding

- Visual inspection is used to sort out dice that may have been damaged during the separation process of inked.
- Each die is then mounted onto individual chip carriers to form a single chip module (SCM).



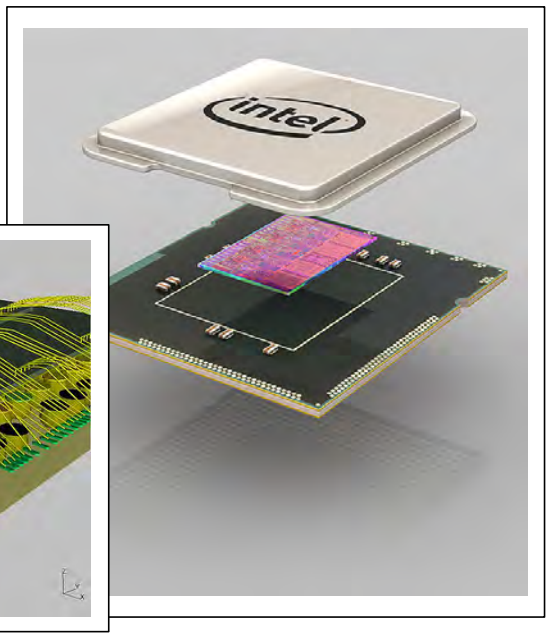
- Epoxy Die Attachment
  An epoxy cement is used to attach the die to the chip carrier. Epoxy is a poor thermal conductor, but a good insulator.

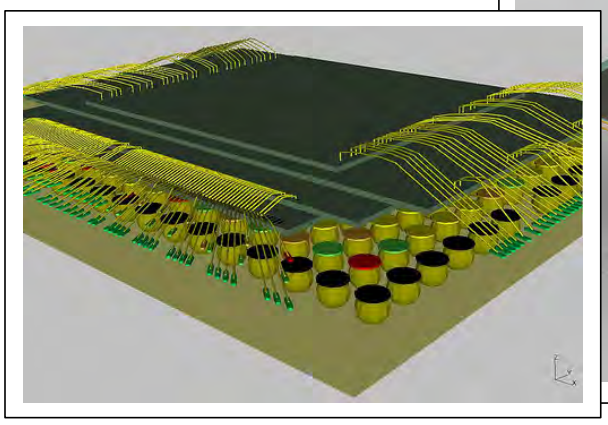
Die attachment

- Alumina can be mixed with the epoxy to increase the thermal conductivity.
- Gold or silver filled epoxies can be used to reduce thermal resistance and to provide a low resistance electrical connection.
- Eutectic Die Attachment:Gold-silicon (3.6% Si and 96.4% Au) has a eutectic temperature of 370°C. Gold can be deposited to the back of the wafer prior to separation. To form a eutectic bond, the die package are heated to 390°C and pressure is applied to the die in conjunction with ultrasonic scrubbing.
- Solder attachment is often used in power devices.

Die attachment (cont'd)

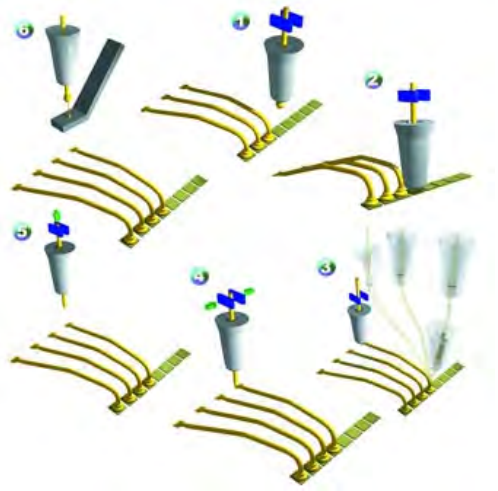
- Modern VLSI packages can have up to a thousand pins and usually require special ball grid array (BGA) packages and very complicated wire-bonds.





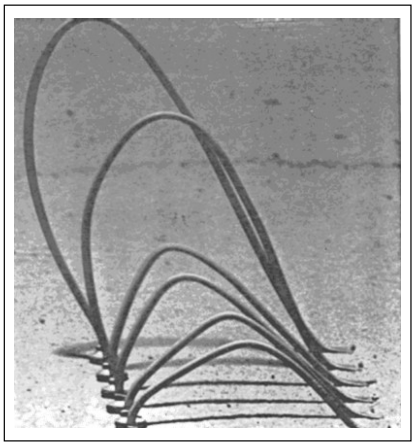
Wire Bonding

- Wire bonding is the most widely used method for making electrical connections between the die and package.
- The bonding areas on the die are large, square pads, 100 to 125μm on a side, located around the periphery of the die.
- Fine wires interconnect the aluminum bonding pads on the IC die to the leads of the package.
- The wire bonding process is very similar to the sewing machine, except that gold wires are used.

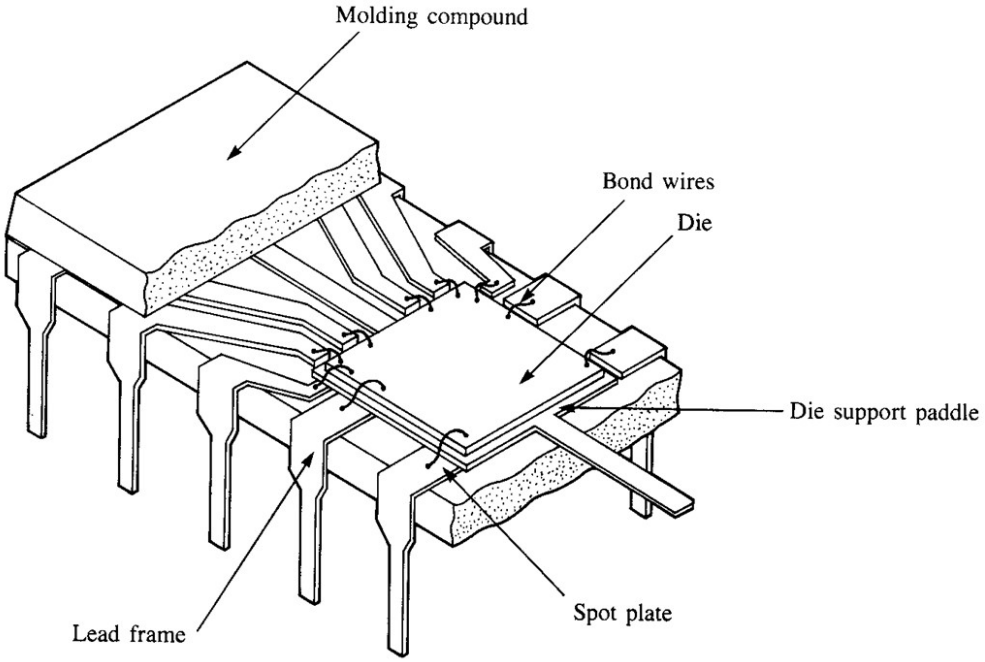


Wire Bonding (cont'd)

- A ball formed by melting the gold wire is positioned over the bonding pad of the die. It is pressed and deformed to form a "nail head".
- The bond-head is then raised and drag the gold wire (from a spool) to a position over the lead of the package.
- The second bond is wedge bonded by deforming the wire with the edge of the bond-head (e.g. ultrasonic scrubbing).
- After formation, the bond-head is raise and the wire is broken near the edge of the bond.

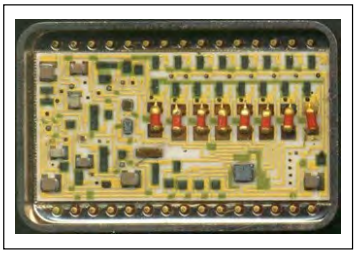


Wire Bonding (cont'd)

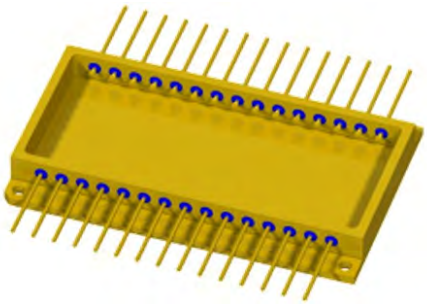


Thick Film and Thin Film Hybrid

- A hybrid circuit is an assembly of both active and passive components interconnected via a substrate made from various material.

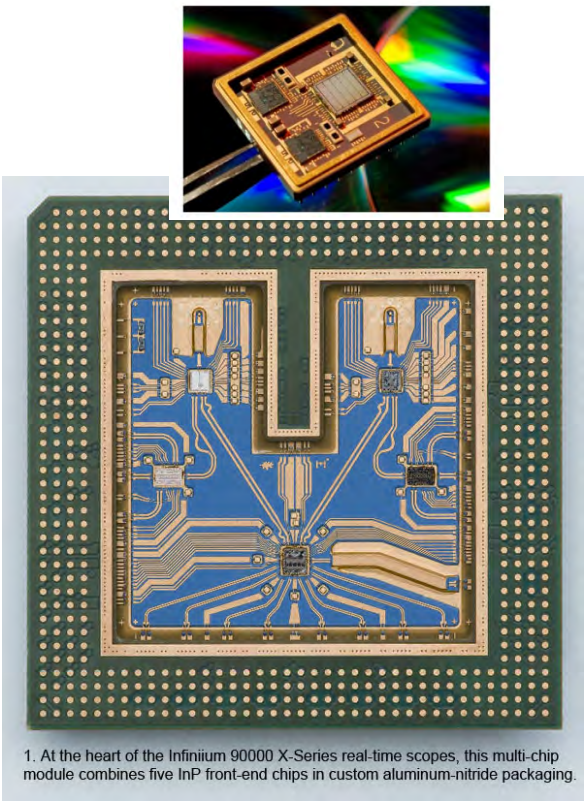


- The interconnection pattern, placement of components and packaging are usually carried out by the manufacturer.
- Hybrid circuits, using thick or thin film substrates can act as an interim solution between a regular printed circuit board and a monolithic IC.



Multi-chip Modules

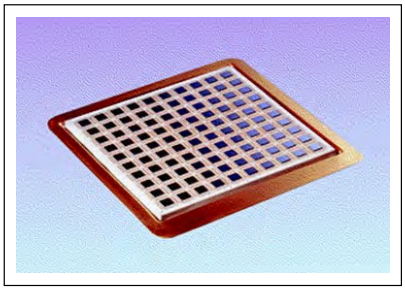
- Since the 1970s, the industry was faced with the need to design faster generation of computers.
- It was clear that to meet performance objectives, not only did the speed of the circuits on the silicon chips have to be improved, but that the delay between the chips had to be reduced significantly.



1. At the heart of the Infiniium 90000 X-Series real-time scopes, this multi-chip module combines five InP front-end chips in custom aluminum-nitride packaging.

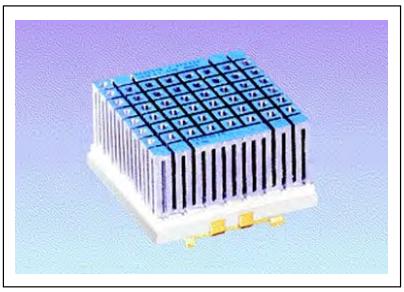
Multi-chip Modules (cont'd)

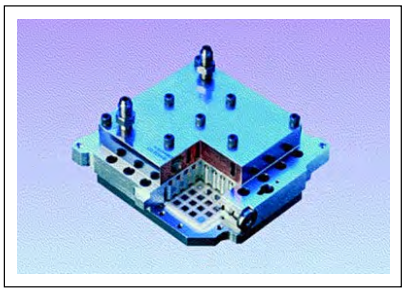
- MCM combines high performance ICs with a custom-designed common substrate structure which provides mechanical support for the chips and multiple layers of conductors to interconnect them.
- This arrangement takes better advantage of the performance of the ICs than does interconnecting individually packaged ICs because the interconnect length is much shorter.
- MCMs are supported by a complex substrate structure which is fabricated using multi-layer ceramics, polymers, silicon, metals, glass ceramics, laminates, etc.



MCM Technology Requirements (cont'd)

- Support High Power Density: metal heat spreader coil can be used to provide a thermal path from the back side of the chip to the heat sink.





- The thermal path is provided by a spring-driven piston. The interior of the substrate was filled with helium, providing both a hermetic environment and an improved thermal path. The assembly, in turn, is connected to a water-cooled cold plate.