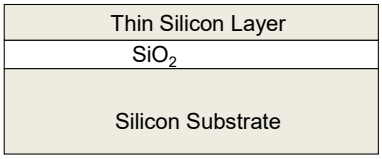
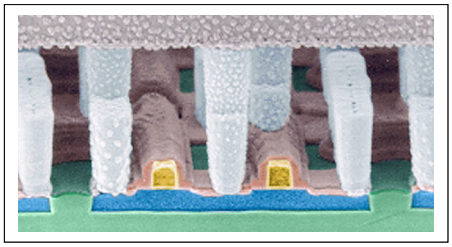
Introduction to SOI

- SOI — **silicon on insulator**, refers to placing a thin layer of silicon on top of an insulator such as SiO_2.
- The devices will be built on top of the thin layer of silicon.
- The basic idea of SOI is to reduced the parasitic capacitance and hence faster switching speed.



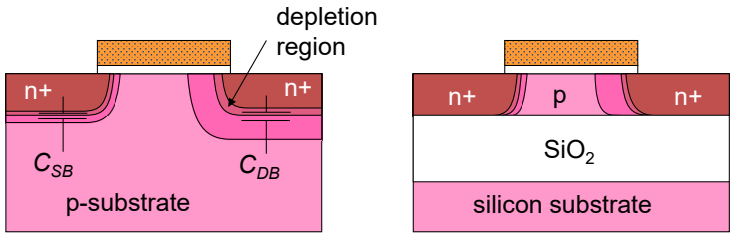


Parasitic Capacitance

- Every time a transistor is turned on, it must first charge all of its internal (parasitic) capacitance before it can begin to conduct.
- The time it takes to charge up and discharge (turn off) the parasitic capacitance is much longer than the actual turn on and off of the transistor.
- If the parasitic capacitance can be reduced, the transistor can be switched faster — performance.
- One of the major source of parasitic capacitance is from the source and drain to substrate junctions.

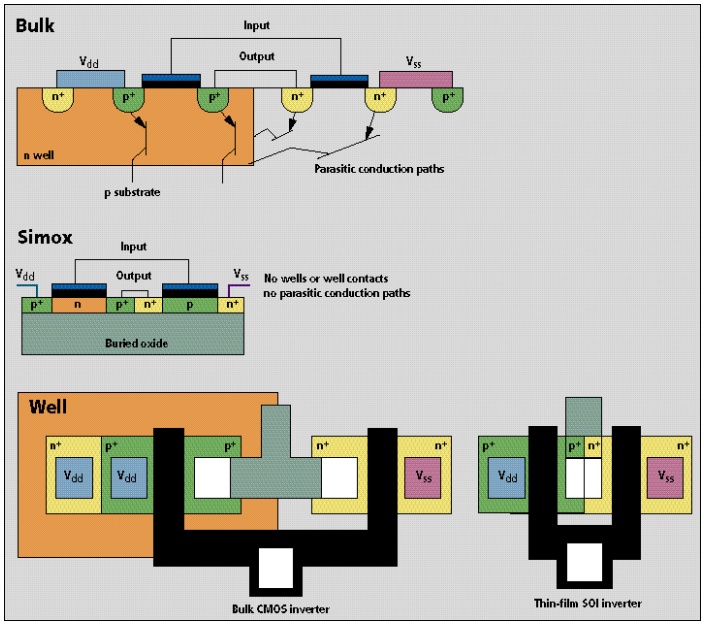
Parasitic Capacitance (cont'd)

- The ultimate goal is to develop a SOI substrate that can be used as the starting material in mainstream CMOS fabrication technology.
- SOI can reduced the capacitance at the source and drain junctions significantly — by eliminating the depletion regions extending into the substrate.



Area Saving

- Comparing the cross sections of inverters fabricated on bulk silicon and SOI substrates, SOI can eliminate the parasitic bipolar devices and latch-up paths in the substrates and reduce circuit size with its simpler isolation structures.

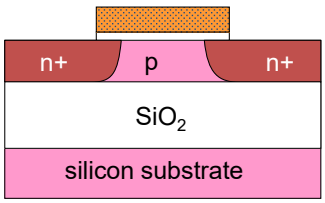


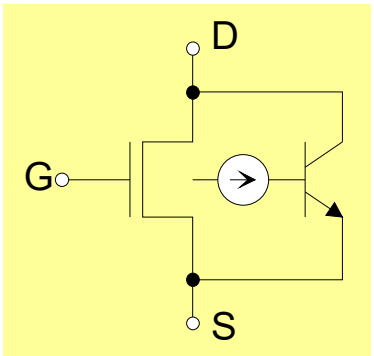
SOI Considerations

- The bulk substrate used for making MOS transistor is a perfect crystalline silicon.
- Since the insulating layer is not crystalline (SiO_2 is amorphous), it is very difficult to grow perfect crystalline silicon on top of it.
- If perfect crystalline silicon is not available, defects will degrade the MOS transistor severely in terms of speed (mobility) and leakage.
- Sapphire was studied briefly as a possible alternative to SiO_2 due to the fact that it is an insulator with a crystalline structure. However silicon on sapphire (SOS) was still found to contain lots of defects.

SOI Considerations (cont'd)

- Besides the material issues, SOI MOS device also poses structural problems. The MOS device is always accompanied by a parasitic transistor connected in parallel.
- Unlike the case in bulk silicon, the base of the bipolar transistor is not connected
  GND. It is floating!!





SOI Considerations (cont'd)

- The bipolar transistor can turn on when the MOS transistor passes current through the channel (base current will be supplied by base impact ionization).
- This problem gives rise to a number of unwanted effects that can complicate the operation of the chip's circuit and device modeling.
- Significant effort has been devoted in the last three decades in characterizing, modeling, eliminating or at least reducing, and controlling the unwanted effects caused by the bipolar devices.
- This leads to the study of "**fully depleted**" and "**partially depleted**" devices.

Choice of Processing Technologies

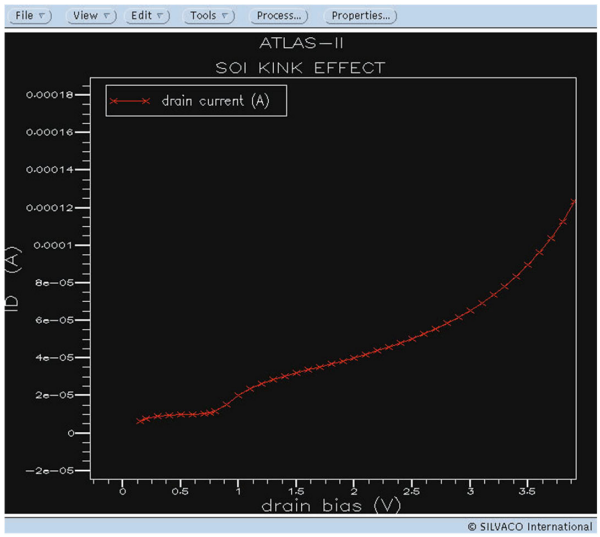
- SOI provides a foundation for many technology options--CMOS, bipolar, and BiCMOS, among others.
- For low-power electronics, the primary candidate is CMOS. Here, thin-film SOI offers the possibility of **fully depleted** operation.
- In such a case, the maximum width of the depletion region beneath the transistor gate is greater than the silicon layer's thickness.
- The entire body of the transistor is depleted except for an accumulated or inverted channel region.

Choice of Processing Technologies (cont'd)

- Such devices are attractive for mainstream CMOS IC evolution for several reasons.
  - they have an ideal subthreshold slope of 60 mV per decade,
  - they are resistant to short-channel effects, and
  - they altogether eliminate the floating-body effects that afflict partially depleted thin-film SOI devices.
- Floating body effects are unique to **partially depleted** devices.
- Because the threshold voltage is modulated by the charging in the isolated transistor body, the effects produce a "kink" in the dc IV characteristics of SOI transistors.

Choice of Processing Technologies (cont'd)

- SOI device IV characteristics with kink effect.



Choice of Processing Technologies (cont'd)

- They reduce the transistors' breakdown voltage and cause hysteresis in the switching characteristics, and their prevention complicates the circuit design.
- The floating-body effect can be addressed in the process integration in several ways, including
  - lightly doped drain and source structures
  - body ties
  - the reduction of minority-carrier lifetime through germanium implantation
  - band-gap engineering
  - the application of substrate bias
  - field-shield isolation.

Choice of Processing Technologies (cont'd)

- The effects are not pronounced in fully depleted devices, where the gate voltage controls the body potential.
- But manufacturing issues present difficulties for fully depleted devices.
- They tend to be more sensitive to material parameters because they use thinner silicon films, while contact formation and threshold voltage control are more challenging.

Choice of Processing Technologies (cont'd)

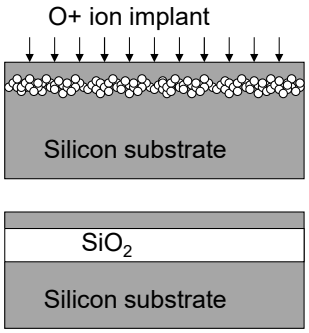
- Several methods of overcoming the sensitivity while maintaining the benefits of fully depleted operation have been shown, such as
  - a near-fully depleted mode of operation
  - threshold doping based on constant doses rather than constant concentration
  - raised source and drain regions.
- There is a tradeoff for CMOS applications: existing designs are more easily transferable to fully depleted devices, while the process technologies is more easily transferable to partially depleted ones.

SOI Wafers

- The idea of building devices on an insulating substrate is not new, in fact it can be traced back to a patent by Heil *et al.* back in 1934.
- However, the availability of practical and economical SOI wafers has been the major obstacle to SOI technology development.
- SOI materials has been successfully introduced in production at the beginning of the 90's for special low volume applications.
- There are different techniques proposed since the 80's to produce SOI wafers, some are compatible to for low voltage CMOS, other are dedicated to PICs.

SIMOX

- **SIMOX** (Separation by Implantation of Oxygen) uses the following key processes
  - An oxygen implantation step using a dedicated machine (100mA, 200keV of O+ ions) to locate underneath the initial silicon surface a high concentration of oxygen.
  - A high temperature anneal to regenerate the crystalline quality of the silicon layer remaining on top of the oxide.
  - This anneal also drives the chemical reaction which forms the oxide buried in the silicon wafer.
  - A last step should be a touch polishing.

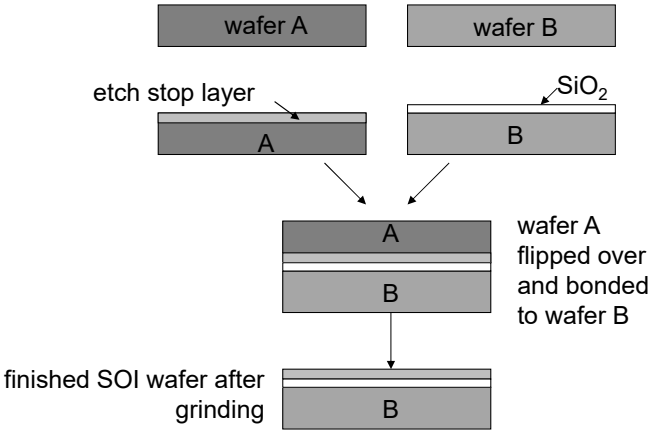


SIMOX (cont'd)

- The new trend in the SIMOX development is the use of low oxygen implantation doses to obtain a low cost SOI material.
- This has drastically improved the top silicon film crystalline quality. However the pin-hole defect density of the buried oxide still needs to be improved.
- The implantation dose is approximately 4×10^{17} O^+/cm^2 limits the buried oxide thickness to 800-1000Å range.
- The main disadvantages of the SIMOX technology is the use of non standard equipment and the need of >1300°C annealing which could be a limitation for 300mm (12") wafer size.

Wafer Bonding

- Direct wafer bonding is an inexpensive technique for manufacturing thick film of both oxide and silicon.
- Starting from two silicon wafers, at least one with an oxide layer on top, these two wafers are bonded together using Van der Walls forces.



Wafer Bonding (cont'd)

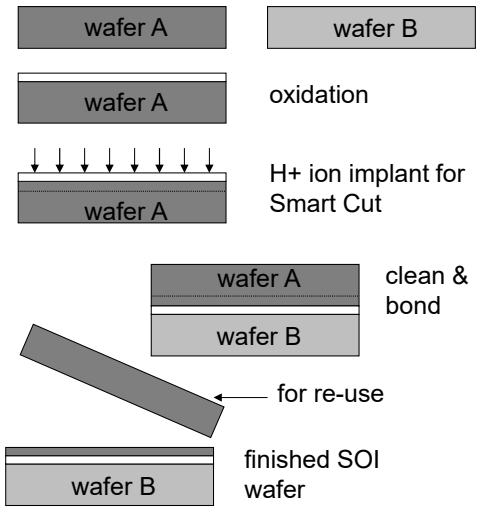
- Subsequent annealing increases the mechanical strength of the bonded interface by the chemical reaction which can occur at this interface.
- One of the substrates is then thinned down to 1μm starting from several 100μm; mechanical grinding and polishing can achieve SOI films of 1μm within 10 to 30% uniformity.
- However, to compete with thin film (e.g. for fully depleted devices), chemical etch stop techniques have been developed.
- Several etch stops have been reported: Boron doped layer, Si-Ge, carbon implanted, and porous silicon.

Wafer Bonding (cont'd)

- However, only a few are compatible with high temperature treatment.
- The uniformity depends on the selectivity of the last etching which varies from 10 to 105, depending on the etch stop.
- To avoid the selectivity problem boron doped technique has been used with a localized plasma etch (RIE).
- Starting from a non-uniform wafer, an accurate measurement of the top silicon film is performed; then a localized plasma etch is used to reduce the variation of the topography.

Smart Cut

- The most recent technique is named Smart Cut. This technology is based both on ion implantation and wafer bonding technologies.
- While the process starts with two wafers, the second wafer is not lost, but recycled to create a second SOI wafer.



Smart Cut (cont'd)

- The ion implantation step assures uniformity of the SOI film. The bonding steps assures use of a thermally grown buried oxide and the perfect crystalline quality of the top silicon film.
- Key equipment used to perform the process are a standard high current implanter and a chemical mechanical polisher (CMP).
- This use of standard equipment is a tremendous advantage to reduce the lead time for capacity increase and to be sure that SOI material will profit from the mainstream improvement to semiconductor manufacturing equipment such as the 300mm wafer.

Smart Cut (cont'd)

- The Smart Cut process:
  - Starting with two wafers, one is oxidized to form what will become the buried oxide layer of the SOI structure.
  - Ion implantation (H^+) through the oxide forms the Smart Cut layer. The dose is in the range of $5\times10^{16}/cm^2$. At this stage only micro cavities or micro bubbles are formed at the straggle range (R_p) of implantation.
  - Both wafers go through a cleaning step (modified RCA) to remove particles and create two hydrophilic surfaces for the bonding to occur.
  - The two wafers are bonded by Van der Walls forces.
  - The top wafer is then cut away using a 500°C thermal activation to form at the implanted R_p a cleavage plane by merging all cavities.

Smart Cut (cont'd)

- The SOI wafer is then annealed at 1100°C
- Finally a touch polishing step finishes the top surface to a roughness <1~5Å. This step could remove a few 100's Å.
- The remaining wafer is reclaimed by the touch polishing process and is used as the support wafer in the next process flow. This wafer is nearly identical in thickness to the original starting wafer.

- The two limitations of conventional bonding are solved by this new technology:
  - First the uniformity for thin SOI layers is obtained as ion implantation is used which is a conformable technique.
  - Second, since the second wafer is saved, the traditional wafer bonding cost barrier to 2X the cost of silicon is no more a limit.

Smart Cut (cont'd)

- As the SOI wafer quality has drastically improved in the last five years the two remaining issues are the capacity and cost.
- The main competition will be between Smart Cut and low dose SIMOX. Both are expected to be priced in large volume production in the same ratio to epi as epi wafer is to prime wafer.
- Therefore SOI will be the next generation of substrate after epitaxy wafer.

Higher Speed and Lower Power

- IC's manufacturers have to face several challenges:
  - the integration of "systems on chip”
  - the continuation of performance improvements which have been linear for 20 years (Moore’s law)
  - and the limited energy supply of the portable systems
- The power consumption is $P \approx C \times V^2 \times f + V \times I_{leak}$ where C is the total capacitance, V is the supply voltage, f is the frequency, and I_{leak} the standby current).
- The supply voltage must be reduced to obtain low power IC's. This power supply reduction has to follow the evolution in battery voltage and capacity.
- The target (SEMATECH road map) is to reach 0.9V using a single battery.

Higher Speed and Lower Power (cont’d)

- However, at such a low voltage, performance is also reduced due to a lower transistor drivability.
- Below 0.5µm generation three strategies for supply voltage appears:

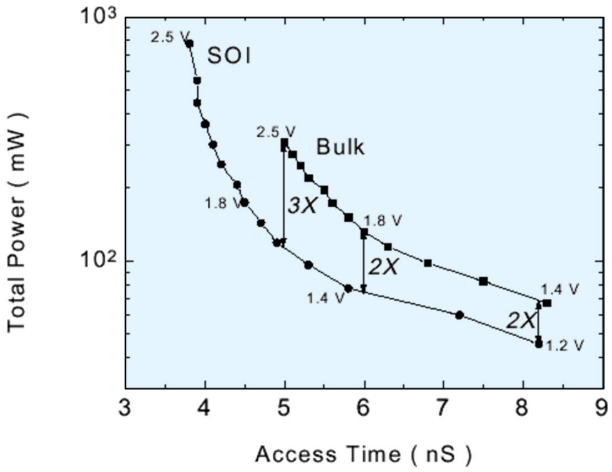
Technology	0.35µm	0.25µm	0.18µm	0.15µm
Standard Design	3.3V	2.5V	1.8V	1.5V
Low Power Design	2.5V	1.5V	1.2V	1V
Low Power SOI	1.5V	1V	0.9V	0.5V

Higher Speed and Lower Power (cont'd)

- The 486 chip of several years ago consumed less than 5W, while a Pentium consumes about 10W, and a 400-MHz Pentium II has peak power consumption of about 28W.
- Increased power seriously limits the use of microprocessors, especially in mobile applications.
- Dropping the voltage is very effective in reducing chip power. The ability of SOI as a low power source originates from the fact that SOI circuits can operate at low voltage with the same performance as a bulk technology at high voltage.

Higher Speed and Lower Power (cont'd)

- As ASIC libraries for SOI are developed, SOI will have a tremendous impact on applications where low power is needed, such as portable and wireless applications.



SOI Advantages

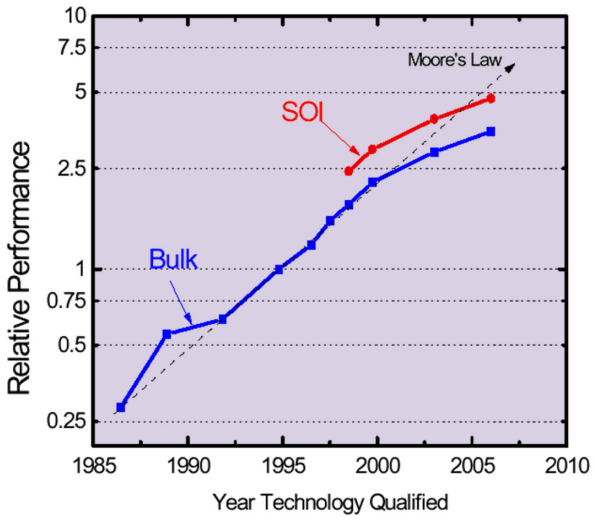
- SOI provides many advantages for low voltage operations:
  - by reducing the junction capacitance thereby inducing a reduction of the total capacitance by 15% to 30% depending on the circuits design;
  - by increasing the switching behavior of the MOS devices (sharper subthreshold slope), allowing a shrink of the threshold voltage thus increasing the current drivability at low voltage and reducing the leakage current;
  - by reducing the junction area at least by two decades, which also decreases the leakage current;
  - by lowering the threshold voltage temperature sensitivity;
  - by suppressing the soft error sensitivity.

SOI Advantages (cont'd)

- by inducing some process simplification, mainly in the isolation and high energy implantation.
- by inducing higher packing density through more aggressive design rules (contact overlap, n+/p+ distance or lateral isolation distance)
- by making easier multi threshold design (MTCMOS) or pass gate logic CPL.
- by offering floating body effects which could act like an elastic VT design.
- by offering new devices for below 0.5V operation like the Bipolar-MOS structure.

SOI Advantages (cont'd)

- Whatever the application, the speed versus power consumption advantage of SOI for low voltage, low power circuits comes from the junction capacitance reduction.



SOI Advantages (cont'd)

- On Moore's chart, SOI will cause a jump in the performance road-map, and will compensate for some of the expected loss of bulk technology performance improvement in the next few years.
- The sources of increased SOI performance are elimination of area junction capacitance and elimination of "body effect" in bulk CMOS technology.
- Body effect is an MOS bulk effect, which results in lower current, and lower performance, in bulk MOS transistors, if they are placed in a certain configuration (i.e. if they are stacked, of if the sources of the MOS devices are not grounded).

SOI Advantages (cont'd)

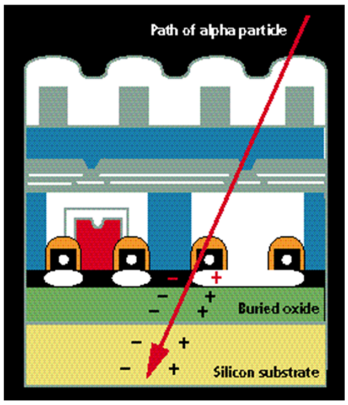
- Threshold management is the most critical issue of the low power, low voltage application.
- Some circuits architectures proposed to modifying the threshold depending on the circuit state: Multi Threshold CMOS (MTCMOS), Pass Gate Logic CPL, Elastic VT.
- SOI devices have an inherent elastic VT as the body of the MOS transistor is floating. In transient the body voltage follows the drain voltage. This has been reported as transient floating body effects.
- The dynamic threshold voltage is lower than the static one which allows low standby current and high speed.

SOI Advantages (cont'd)

- Floating body can be suppressed in the analog part of the circuits by source drain engineering.
- Implantation of Nitrogen or Germanium in the source drain region allows a band gap reduction in favor of lower floating body effects.
- The use of body contacts is an other way to suppress such effects.
- SOI also offers a unique way to control the threshold voltage. By connecting the floating body and the gate a quasi ideal subthreshold slope is obtained with very low V_{TH}.

Soft Error Rate

- Soft errors in memories are typically caused by an alpha particle--the nucleus of a helium atom--that penetrates the silicon and creates excess charge by ionizing the atoms in its path.
- Some of this charge may be collected by the storage node, and if enough is collected, the value of the stored data could change.



Soft Error Rate (cont'd)

- In an SOI-based dynamic RAM cell, the buried insulating layer truncates the collection region so that the storage node cannot accumulate enough charge to change the cell's logic state.

Conclusions — The Hurdles Ahead

- Substrate quality, cost, and availability have improved noticeably in the past three years, but the consistency and cost of materials and their availability in large volumes remain problems.
- Probably, the availability of large quantities of wafers--particularly wafers of the same material from multiple sources--will have to be addressed, too.
- Circuit design is another bottleneck: design tools for large circuits are not widely available for thin-film SOI devices.

Conclusions — The Hurdles Ahead (cont'd)

- The unique floating-body effect makes design difficult without accurate models, but the models are more complex and do not lend themselves to large circuit designs.
- Even with good design tools, large circuit designs can require tremendous resources. Ways of dealing with the floating-body effect demand added process steps or circuit area, thus reducing thin-film SOI's benefits.
- None of these problems looks like being a permanent obstacle for thin-film SOI, but the money and time needed to overcome them leave the momentum at present to bulk-silicon technologies.

Conclusions — The Hurdles Ahead (cont'd)

- For many years, thin-film SOI was thought of as a technology of the future. But the past decade, developments indicate that the future is in sight. Much of the research on thin-film SOI at universities and research institutes has been transferred to industry.
- SOI is a key technology on the Semiconductor Industry Association's road map of the 21st century.
- For thin-film SOI, it seems a question, not of if, but of when--and of who will be first to market.
- Several major semiconductor manufacturers are proceeding in this direction, and their success will be critical in determining whether thin-film SOI will be a standard technology for the IC industry.

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