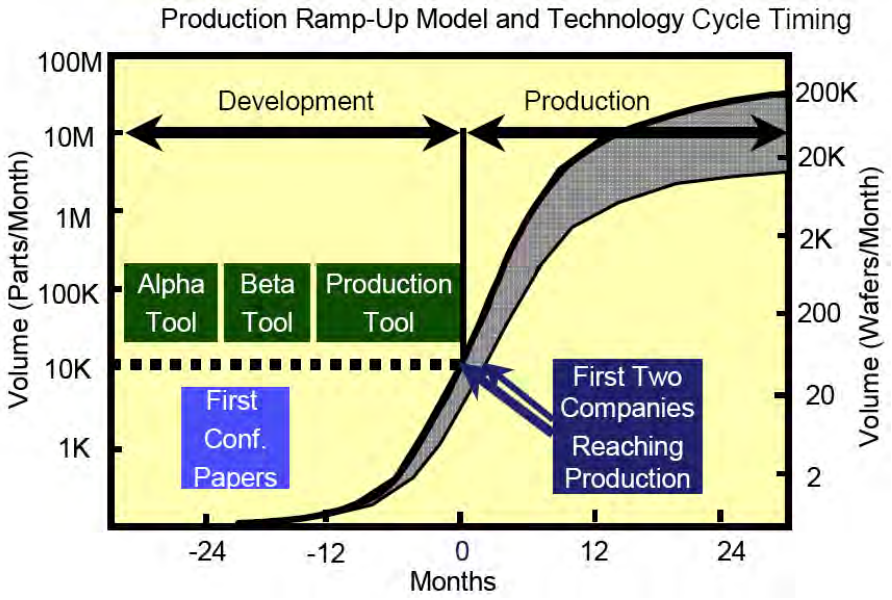
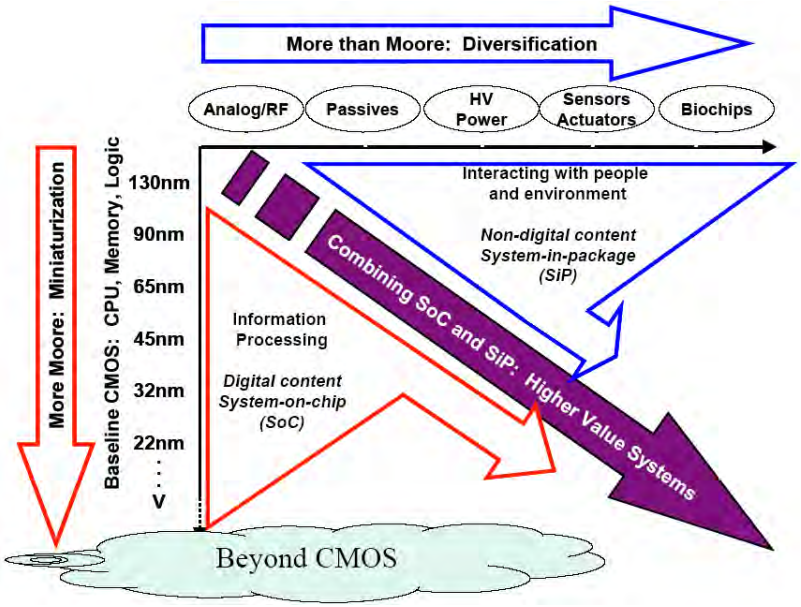
Typical Production Ramp

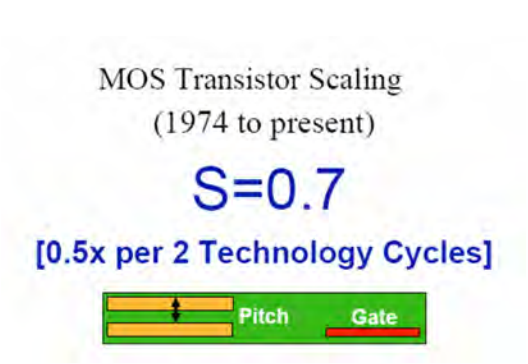


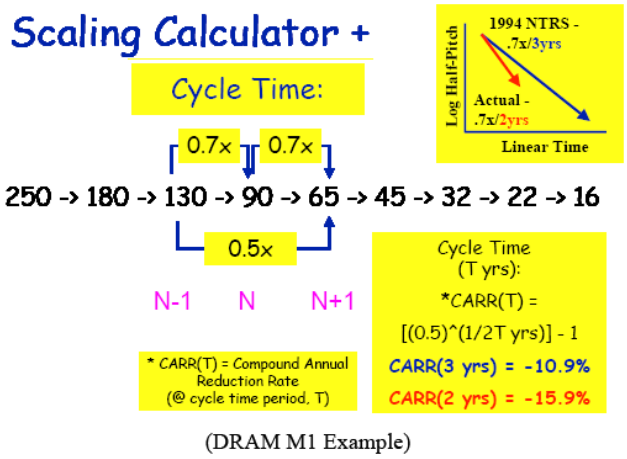
More Than Moore



MOS Transistor Scaling

- 1974 to 2010-ish





(DRAM M1 Example)

Key Technical Innovations

- Self-aligned source/drain and low voltage operation — reduce parasitic and hot-carrier effect
- Deep UV lasers — push lithography to below 0.25µm
- CMP (chemical-mechanical polishing) — replaces LOCOS by shallow trench, increases number of interconnection levels

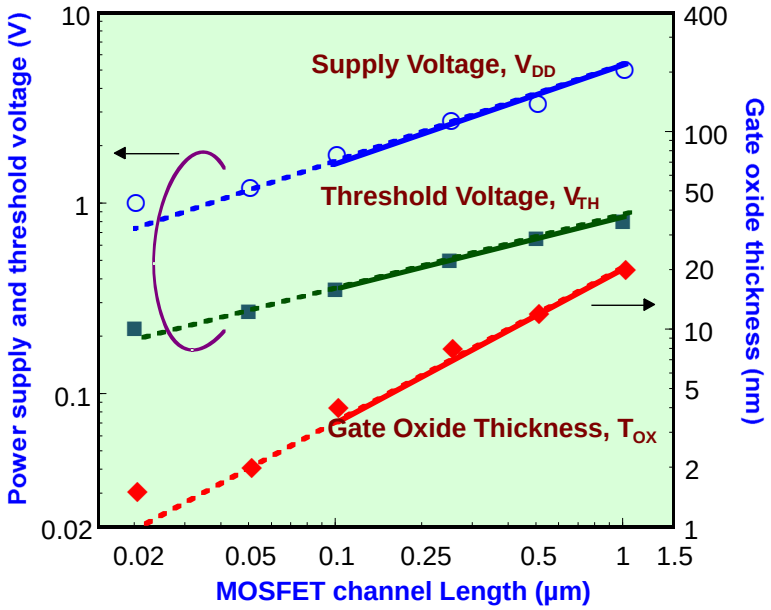
Major Challenges

- How long can the microelectronic industry maintain this trend?
- Fundamental challenges:
  - Lithography
  - Device
  - Interconnect
- Practical challenges:
  - Design capability and knowledge
  - Critical dimension control
  - Reliability

Deep Sub-micron CMOS

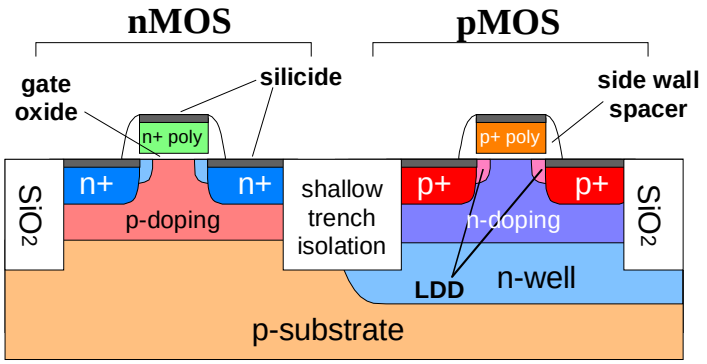
- Non-scalable sub-threshold, lower V_{TH} and V_{DD}
- Tunneling in thin gate oxide (~2nm)
- Doping fluctuation on device characteristics
- New device structures
  - Double gate ultra-thin MOSFET (L=17nm)
  - Single electron transistors
  - Neuron devices
- New material to extend device miniaturization
  - Low k and high k dielectrics
  - Electrode materials (e.g. Cu)
  - Ferroelectrics

Voltages and Gate Oxide Thickness

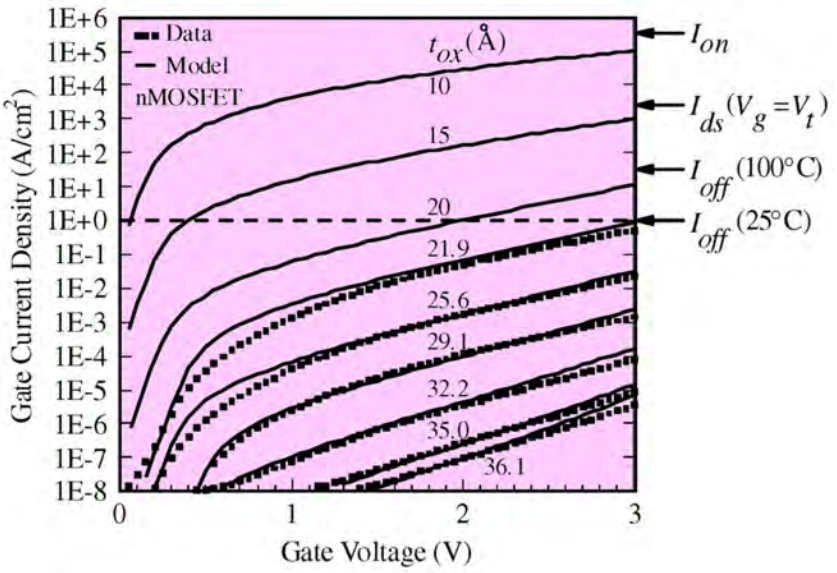


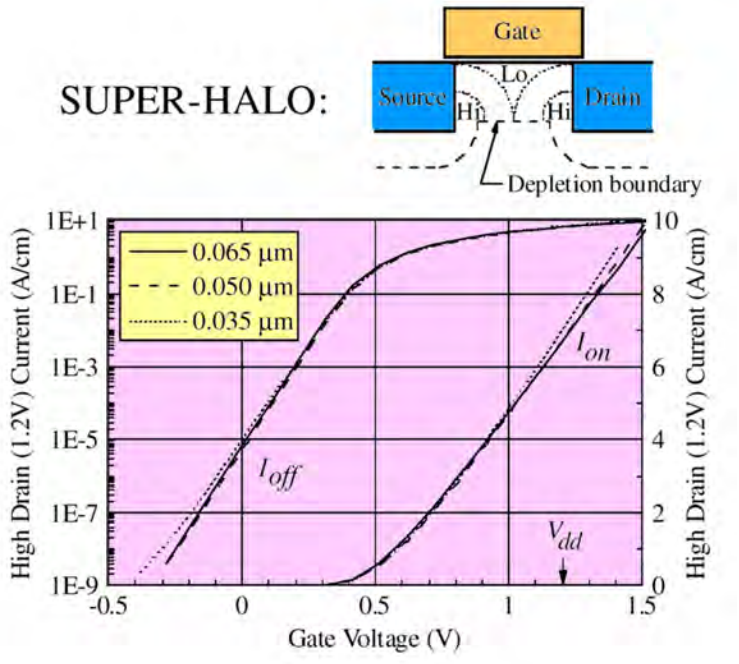
Advanced CMOS

- CMOS devices in 0.10 - 0.13μm lithography range will feature: shallow trench isolation, 1.5 - 2.0nm gate oxide, n+ and p+ doped poly gate, 30 - 50nm LDD, and self-aligned silicide for contacts.



Gate Leakage for various Oxide Thickness





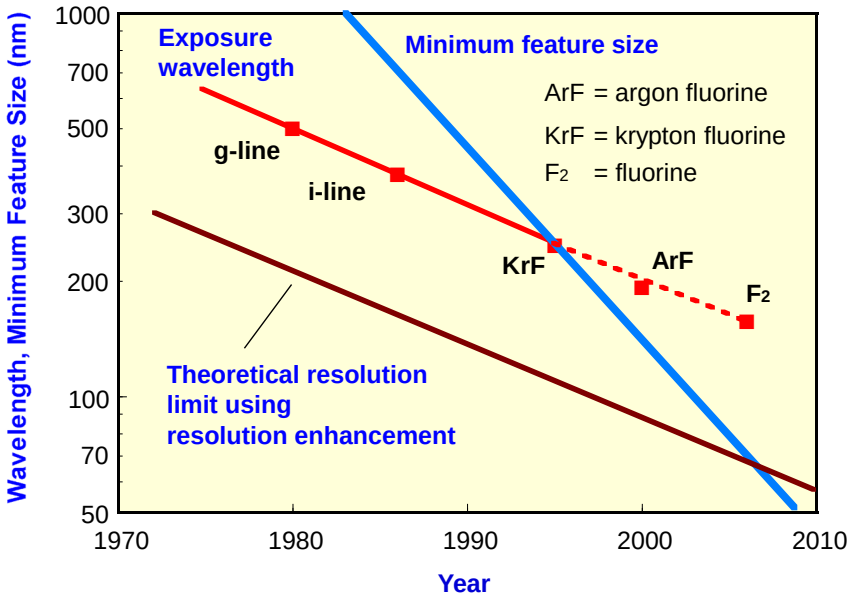
Future Device Parameters

- V_{TH} will not likely to scale below 200mV due to subthreshold leakage. V_{DD} will remain at around 1V.
- A rule of thumb for scaling gate oxide is that T_{ox} = 1/50 to 1/25 of the channel length. For 0.10 - 0.13µm, a 1 - 2nm thick gate oxide is needed.
- Thin gate oxide (a few atomic layers thick) is vulnerable to quantum-mechanical tunneling — more leakage.
- Doped poly gates are needed to reduced V_{TH} to below 300mV for the n and p-MOSFETs.
- Channel profiles will be both vertically and horizontally non-uniform (Super Halo).

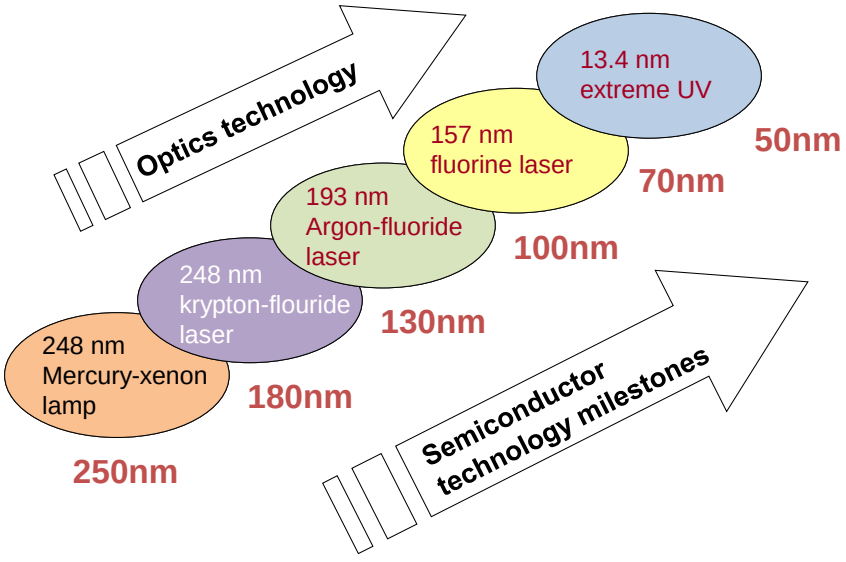
Ultra High-Resolution Lithography

- Leading edge production lithography employs optical projection printing operating at the conventional Raleigh diffraction limit (g-line and I-line)
  g-line = 436 nm wavelength UV
  i-line = 365 nm wavelength UV
- Excimer lasers (KrF) produce light in the deep UV spectrum (248nm) and are used in 0.25µm CMOS.
- Resolution enhancement technology such as phase-shift masks can control the amplitude and phase of the light at the image plane. This allow features at half of the wavelength be printed (theoretically).
- Optical printing systems cannot keep up with the rapidly shrinking transistor size (cross over at 2008).

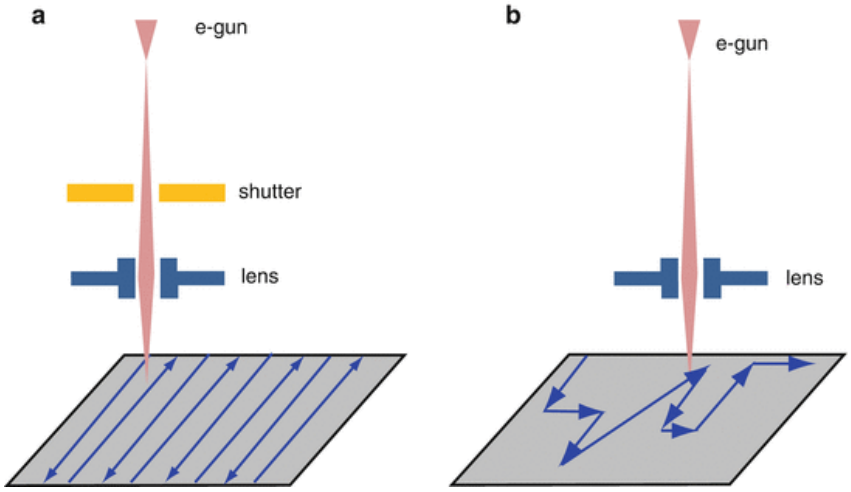
Optical Lithographic Systems



Progression Toward Shorter Wavelengths



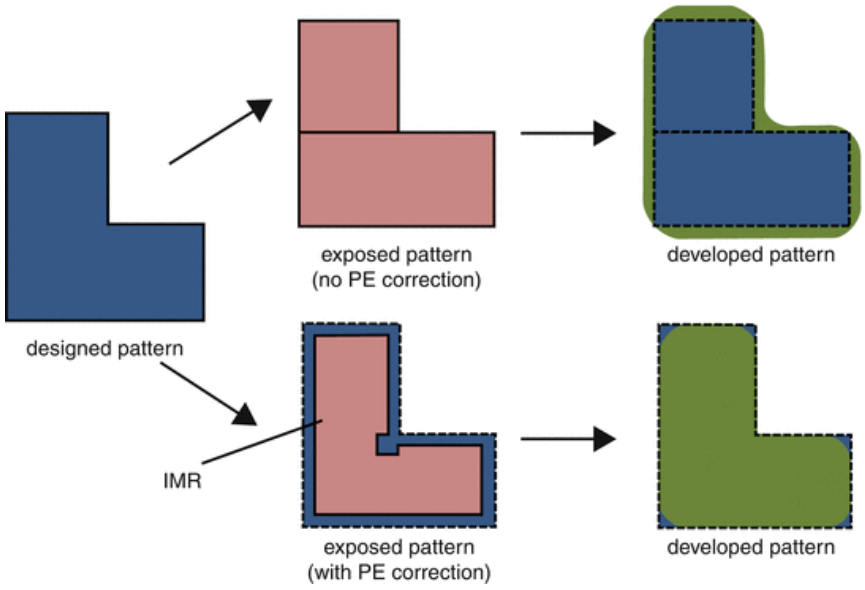
Electron Beam Lithography (EBL)



Raster Scan Vector Scan

https://link-springer-com.myaccess.library.utoronto.ca/referenceworkentry/10.1007/978-90-481-9751-4_344

Proximity-Effect Correction

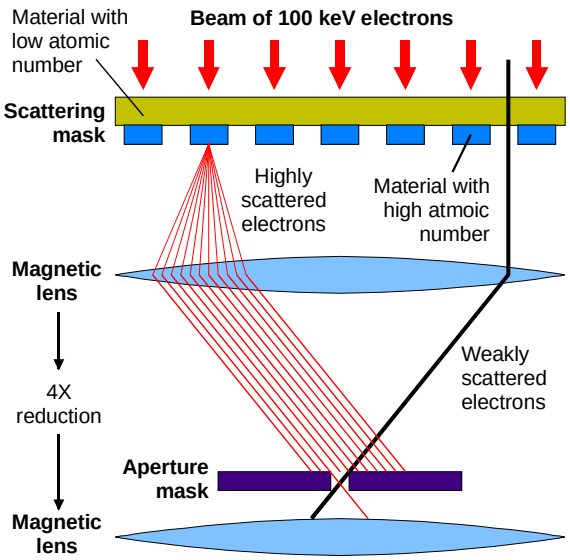


https://link-springer-com.myaccess.library.utoronto.ca/referenceworkentry/10.1007/978-90-481-9751-4_344

Scalpel

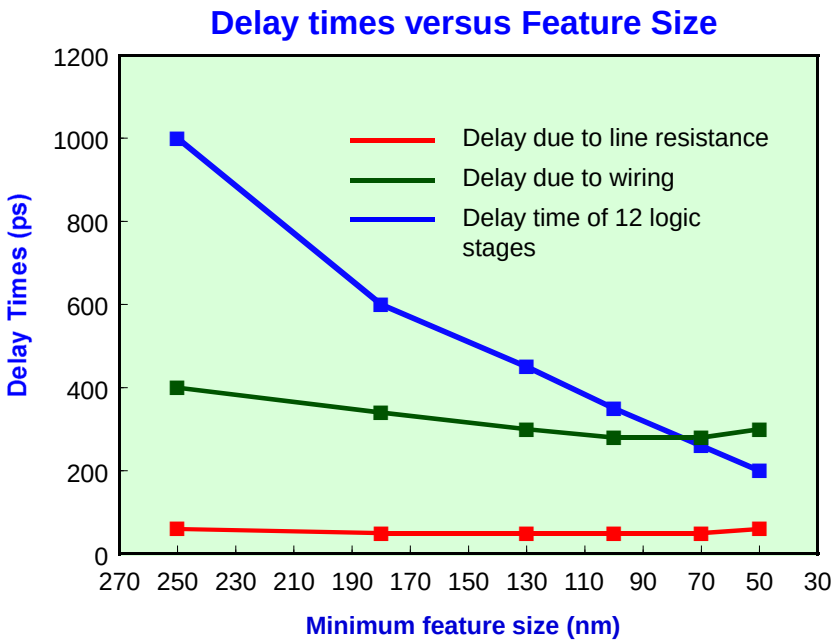
- **Scalpel** — **SC**attering with **A**ngular **L**imitation **P**rojection **E**lectron-beam **L**ithography.
- A reduction imagine projection technique relying on the contrast caused when they are scattered.
- The high energy electron-beam is scattered weakly by the membrane mask which is almost transparent. The electrons are scattered strongly by the masking pattern.
- An aperture mask blocks the strongly scattered electrons, forming a high-contrast image at the wafer surface.

Scalpel



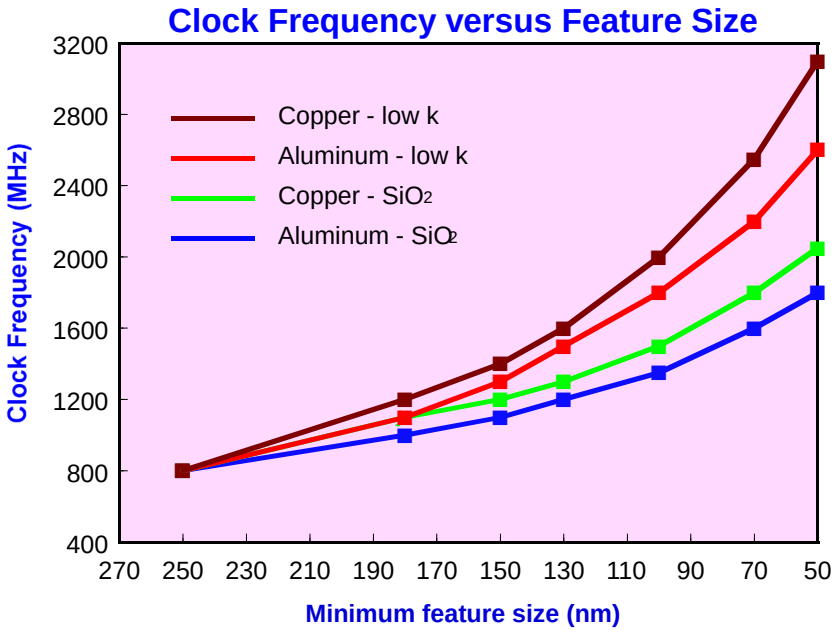
Interconnection

- The most prominent microprocessor parameters is the clock frequency.
- Pushing it above 1GHz will require not just a simple scaling of the devices to smaller sizes, but also interconnects and packaging changes.
- Shrinking feature size can lead to shorter gate delay and interconnect delay since the logic gates are closer together.
- However, as the signal lines continues to get narrower, the interconnect delays become a significant percentage of the overall delay.



Interconnection (cont'd)

- Below 0.25µm, the narrow signal lines have significant resistive loss and the current density is reaching the electromigration limits.
- These lines are often 0.5 to 1µm thick, resulting in large parasitic capacitance when closely spaced.
- Current manufacturers are replacing all or some interconnect lines from aluminum to copper.
- Copper has a lower resistivity, about 2µΩ·cm compare to 4µΩ·cm for aluminum.
- More importantly, copper has a electromigration limit that is an order of magnitude higher then that of aluminum.



Interconnection (cont'd)

- Line to line capacitance can be reduced by narrowing the copper lines while keeping the same spacing as the aluminum interconnects.
- Once the copper transition is achieved, the next problem will be to substitute the insulating films with low dielectric constant, k.
- IBM, Motorola, Texas Instruments, Intel, and AMD, etc. are exploring the use of low k (<2) to replace SiO_2 (k = 3.9).
- Low k material are typically organic insulators, with lower processing temperature, lower mechanical strength, and lower thermal conductivity than SiO_2.

Interconnection (cont'd)

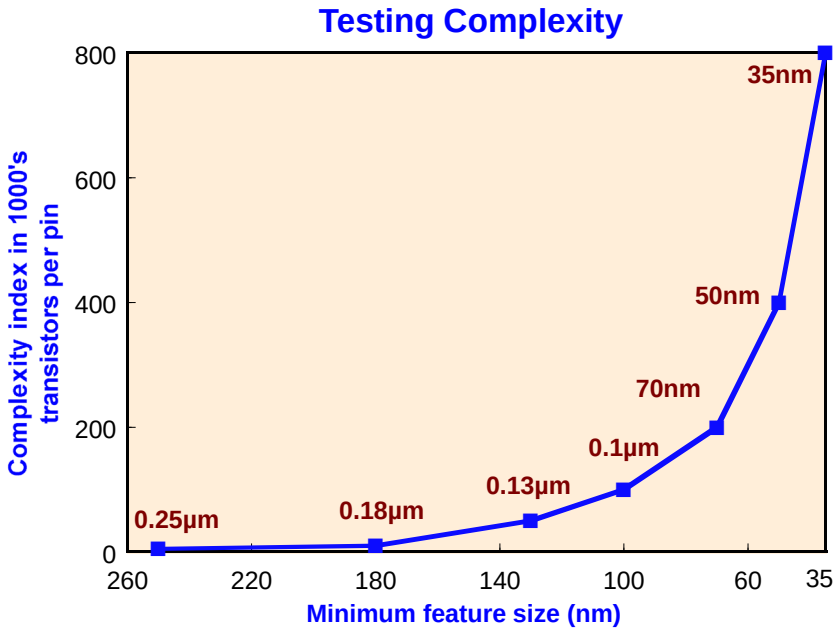
- Two significant process changes are underway that will get the industry into the super-gigahertz regime:
  - Al- SiO_2 will be replaced by copper-low k systems
  - For long signal lines, repeaters will be used
- In addition, changes will also take place in transistor level circuit design to make the logic gate better long-line drivers.

VLSI Design

- By 2005, scaling supply voltage down to <1V will result in at least 10 of today's µPs fitted into a single chip.
- VLSI design is traditionally driven by µP designs: interconnects, storage, logic circuits, performance, and productivity.
- With the impending requirement to design large chips, designers must advance their art: handling rapidly changing currents, optimization, asynchronization, reuse, and managing design skills.

Complex Device Models

- Once upon a time, the driver device could be viewed as a resistor in series with a switch and a current source with the load a capacitive load.
- The current can be considered as switching ramps.
- In deep sub-micron designs, designers will be faced with modeling distributed loads with coupling to many other switching elements.
- Drivers will have nonlinear output impedance, current supplied through an inductive power grid, and receiver with a narrow window of switching threshold.



Design for Testability

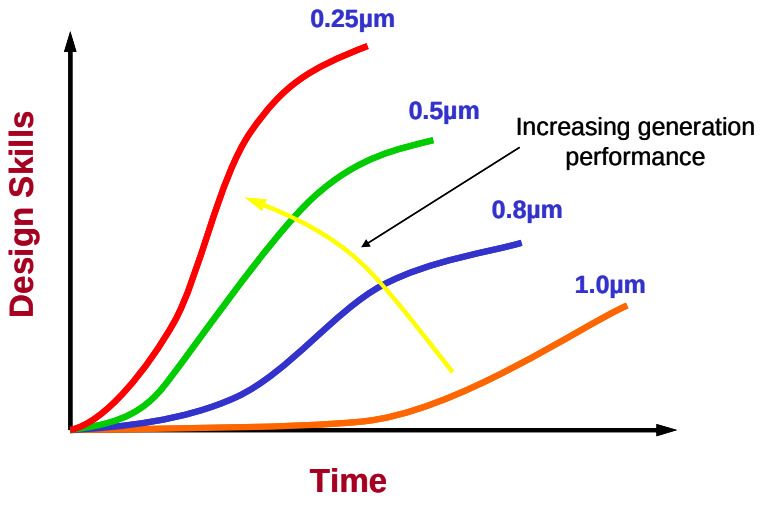
- Since the number of transistor per chip raises much more rapidly than the number of pins per package, exhaustive testing of all devices is impossible.
- Limited I/O posses not only access difficulties, the growing differences between internal clock and output capability of I/O ports makes full speed testing extremely difficult.
- The widening gap between external and internal bandwidth is the main reason why processors and DRAMs are now being integrated together to form Systems-on-Chip (SOC).

Design for Testability

- SOC design based on embedded cores implies reuse of previously design and tested complex functional blocks.
- SOC with more test-friendly cores would simplify the task of integration.
- With the next generation of VLSI having a transistor to pin ratio exceeding 1000:1, testing depending on external test equipment is out of the question.
- Embedded test circuits must be integrated all future designs.

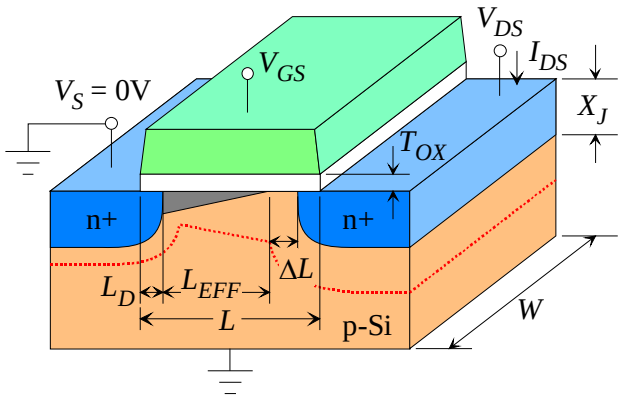
Design for Testability

- A steeper ramp up for VLSI development is required for every new generation.



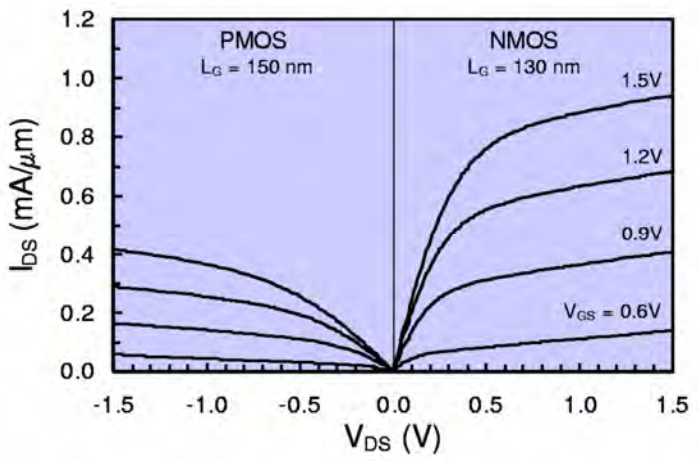
Short Channel Effects

- Short channel effects are more apparent when the channel length L is comparable to the junction depth X_J of the source and drain diffusion.



Short Channel Effects

- One of the distinctive feature of the IV characteristics for short channel device is that the drain current increase with V_{DS} — large g_{ds}.



Channel Length Modulation

- The depletion-layer under the n^+ drain junction is a function of V_{DS}. Assuming an abrupt junction,

$$x_d = \sqrt{\frac{2\varepsilon_s\varepsilon_0(\phi + V_{DS})}{qN_{SUB}}}$$

- The depletion charge is

$$Q_d = -qx_dN_{SUB} = -\sqrt{2q\varepsilon_s\varepsilon_0N_{SUB}(\phi + V_{DS})}$$

- The depletion-layer extends both vertically and horizontally. The horizontal (or lateral) extension reduces the channel length by a length of ΔL.

Channel Length Modulation (cont'd)

- Since the depletion layer depends on V_{DS}, the effective channel length also varies with V_{DS}.

$$\Delta L = \sqrt{\frac{2\varepsilon_s\varepsilon_0}{qN_{SUB}}}\left(\sqrt{\phi + V_{DS,sat} + \Delta V_{DS}} - \sqrt{\phi + V_{DS,sat}}\right)$$

where $V_{DS,sat}$ is the voltage at which the device first enters the saturation region.

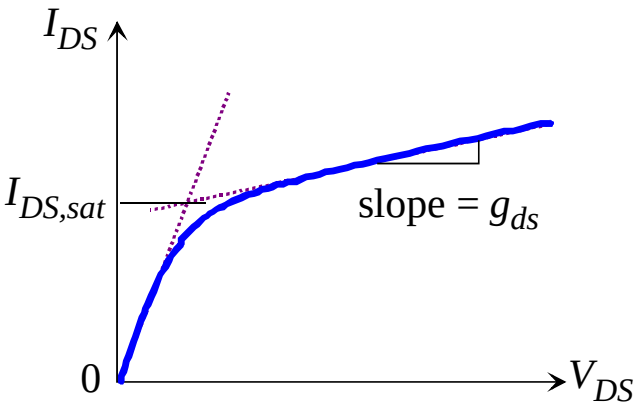
- As the effective channel length reduces and the drain current increases

$$L_{eff} = L - \Delta L$$

$$\frac{I_{DS}}{I_{DS,sat}} = \frac{L}{L_{eff}} = \frac{L}{L - \Delta L}$$

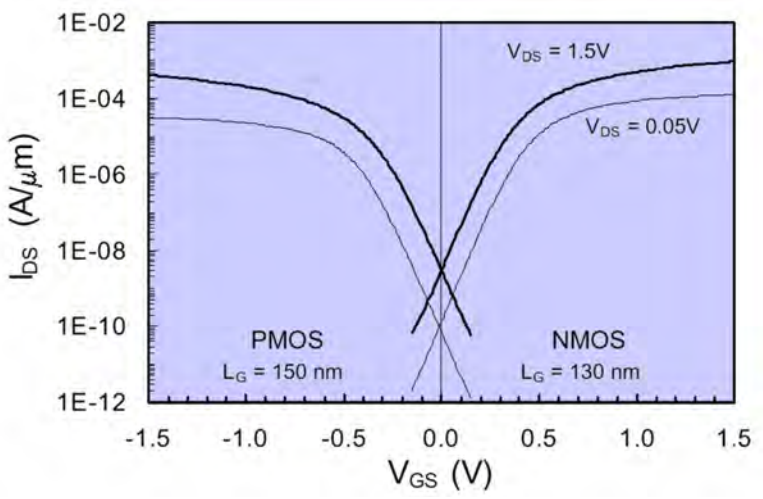
Channel Length Modulation (cont'd)

- $I_{DS,sat}$ is the drain current at the onset of saturation, with $V_{DS} = V_{DS,sat}$
- The output conductance (important in determining the gain), g_{ds} is the slope of the IV curve.



Subthreshold Conduction

- Substantial leakage current occurs for short L. The subthreshold current varies exponentially with V_{GS}.



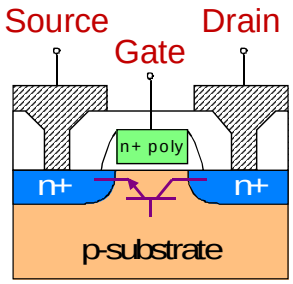
Subthreshold Conduction (cont'd)

- As the channel length reduces, the parasitic bipolar transistor behavior starts to dominate.
- Subthreshold current is caused by carrier diffusion from source to the drain.

where $I_{sub} = I_s(e^{-qV_{SB}/kT} - e^{-qV_{DB}/kT})$

$$I_s = \frac{\mu_n W C_{ox} \gamma (kT/q)^2}{2\sqrt{\psi_{sw}} L} e^{q(\psi_{sw} - 2\phi_f)/kT}$$

$$\psi_{sw} = \left[-\frac{\gamma}{2} + \left(\frac{\gamma^2}{4} + V_{GB} - V_{FB} \right)^{1/2} \right]^2$$



$$\gamma \equiv \frac{\sqrt{2q\varepsilon_s\varepsilon_0 N_{sub}}}{C_{ox}}$$

Threshold Voltage Variations

- The threshold voltage does not remain constant if the dimensions of L and W are reduced.
- The equations developed previously are based on the fact that all the depletion charge is due to the gate bias.

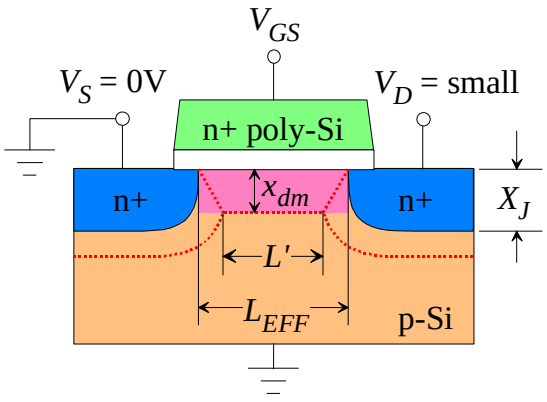
$$V_{TH} = \Phi_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2\phi_F$$

- The total charge contributing to the inversion under the gate terminal is $Q_{bulk} = W' \times L' \times Q_d$
- This is calculated based on a rectangular geometry, without taking account for the influence due to the depletion region from the source and drain.

Threshold Voltage Variations (cont'd)

- Assuming that part of the depletion charge is shared by the source and drain depletion regions, the geometry should be trapezoidal (not rectangular).

$$Q'_{bulk} = Q_d W \frac{L_{EFF} + L'}{2}$$



Threshold Voltage Variations (cont'd)

- Comparing to Q_{bulk}, it is important to determine the factor $L_{EFF} + L'/2L_{EFF}$, which can be proved to be

$$\frac{L_{EFF} + L'}{2L_{EFF}} = 1 - \left(\sqrt{1 + \frac{2x_{dm}}{X_J}} - 1 \right) \frac{X_J}{L_{EFF}}$$

The proper equation for the threshold voltage is now a function of L_{EFF}, X_J, and N_{SUB}.

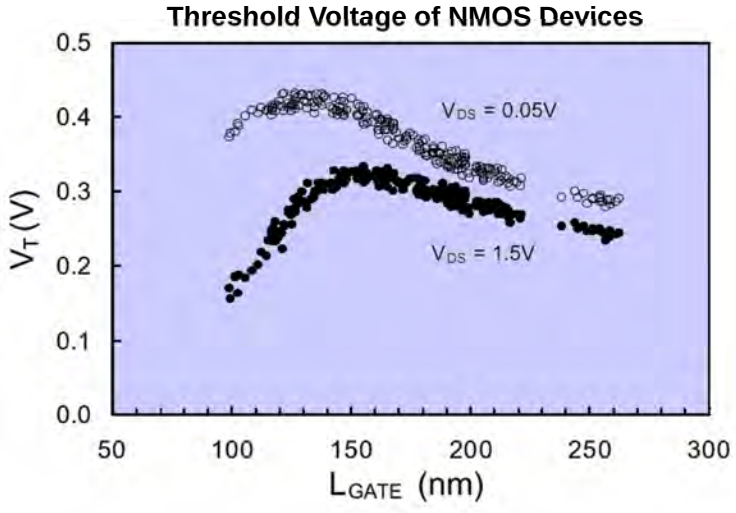
$$V_{TH} = \Phi_{ms} - \frac{Q_i}{C_{ox}} + 2\phi_F - \frac{Q_d}{C_{ox}} \left[1 - \left(\sqrt{1 + \frac{2x_{dm}}{X_J}} - 1 \right) \frac{X_J}{L_{EFF}} \right]$$

Threshold Voltage Variations (cont'd)

- Similar analysis for narrow *W* devices can also lead to an expression for threshold voltage is a function of *W*, X_J, and N_{SUB}.
- If V_{DS} is large, the depletion region will no longer be a trapezoid, but instead will become a polygon. In this case, the threshold voltage will also be a function of V_{DS}.

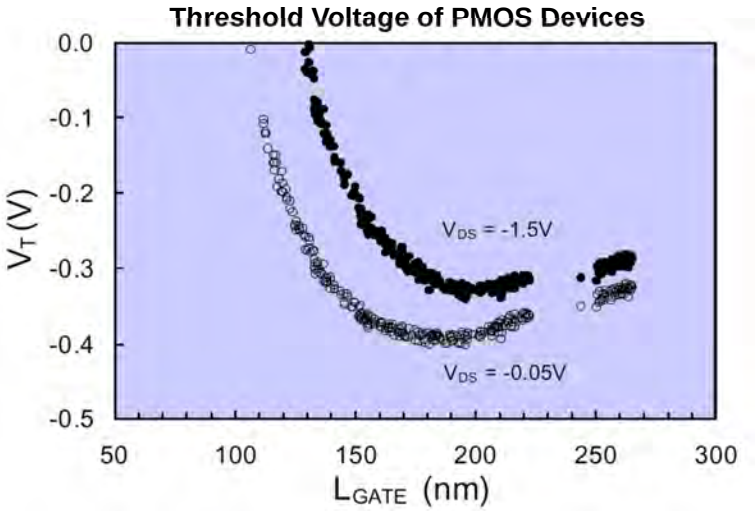
Threshold Voltage Variations (cont'd)

- The threshold voltage V_{TH} is as a function of the channel length *L*.



Threshold Voltage Variations (cont'd)

- As the channel length reduces, the threshold voltage V_{TH} approaches 0V.



Taking Silicon to the Limit

Challenges and Opportunities

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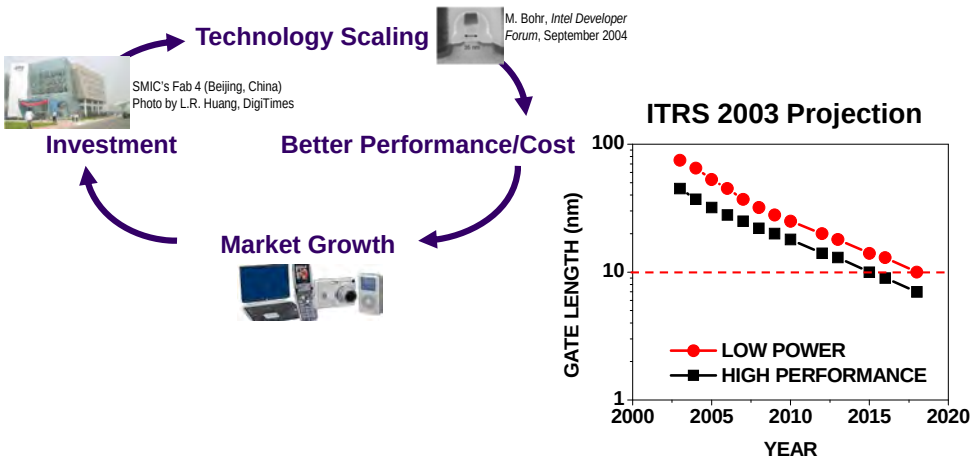
October 19, 2004

Outline

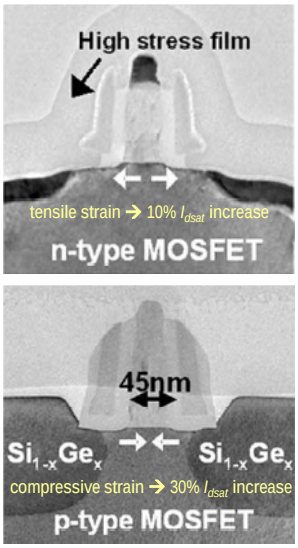
- Introduction
  - ITRS 2003
  - Challenges for MOSFET scaling
- Thin-body transistor structures
- Advanced CMOS materials
- Performance enhancement approaches
- Summary

IC Technology Advancement

Rapid advances in IC technology have been achieved largely by scaling down transistor lateral dimensions



Intel's 90 nm CMOS Technology



T. Ghani *et al.*,
presented at the *Int'l Electron Devices Mtg.*
(San Francisco, CA) Dec. '03

Used for volume manufacture of Pentium® and Intel®Centrino™ processors on 300 mm wafers

- **L_g = 45 nm**
- **T_{ox} = 1.2 nm**
- **Strained Si channel**

Taking Silicon to the Limit
Challenges and Opportunities

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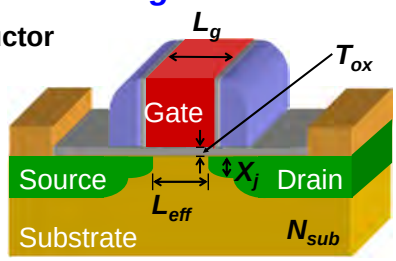
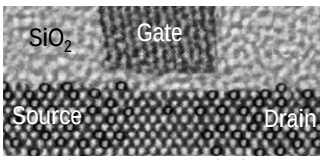
October 19, 2004

Issues for Scaling L_g to <20nm

Metal-Oxide-Semiconductor Field-Effect Transistor:



- **Leakage**
  - drain current
  - gate current
- **Incommensurate gains in I_{dsat} with scaling**
  - limited carrier mobilities
  - parasitic resistance
- **V_T variation**



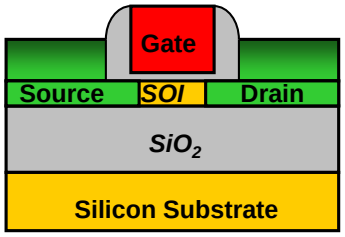
A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002

Outline

- Introduction
- Thin-body transistor structures
  - Ultra-thin-body (UTB) MOSFET
  - Double-gate (DG) MOSFET
  - Back-gated UTB FET
- Advanced CMOS materials
- Performance enhancement approaches
- Summary

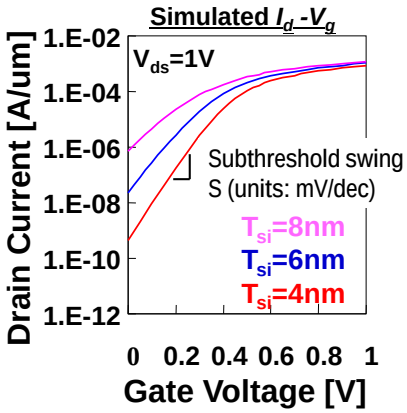
Ultra-Thin-Body MOSFET

- **UTB suppresses leakage**
- **Thick S/D => low R_{series}**

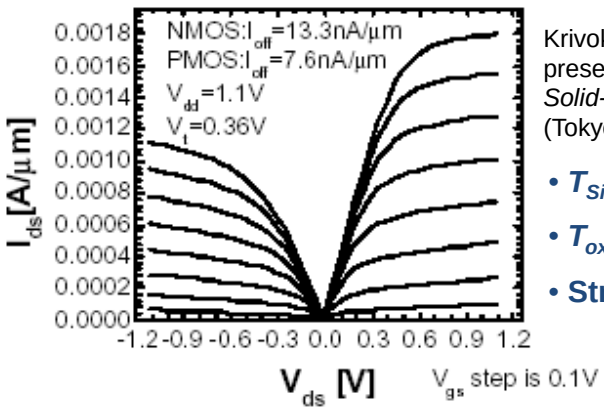


M. Takamiya *et al.*, *Proc. 1997 ISDRS*, p. 215
B. Yu *et al.*, *Proc. 1997 ISDRS*, p. 623

- L_g = 12 nm
- T_{ox} = 2 nm



20 nm L_g UTB CMOSFETs



Krivokapic *et al.* (AMD), presented at the *Int'l Conference on Solid-State Devices and Materials* (Tokyo, Japan) Sep. '03.

- **T_{Si} = 6 nm**
- **T_{ox} = 1.3 nm (SiO_2/Si_3N_4)**
- **Strained Si channel**

- **High I_{dsat} is achieved with thick S/D structure**

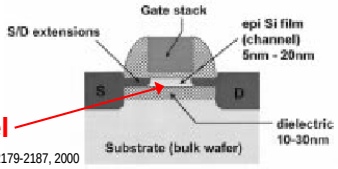
UTB MOSFET Scaling

- Issues for bulk-Si MOSFET scaling eliminated
  - Body does not need to be heavily doped
  - T_{ox} does not need to be scaled as aggressively
- Body thickness must be less than ~1/3 x L_g
  - Formation of uniformly thin body is primary challenge
  - For T_{Si} < 4 nm, quantum confinement & interface roughness → V_T variation and degraded g_m

K. Uchida *et al.*, *IEDM Technical Digest*, pp. 805-808, 2002

→Scaling limit may be $L_g \cong$ 12 nm, unless uniformly thin T_{Si} and atomically smooth interfaces are achieved, *e.g.* by epitaxial growth of the Si channel

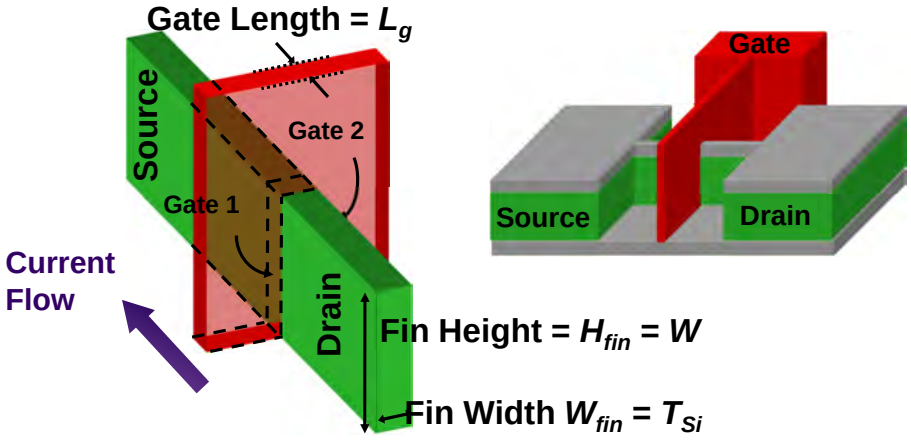
"Silicon on Nothing" Process



M. Jurzcak *et al.*, *IEEE Trans. Electron Devices*, pp. 2179-2187, 2000

Double-Gate "FinFET"

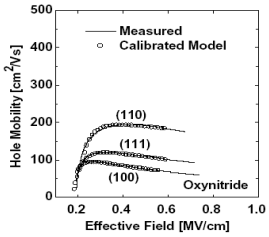
- **Self-aligned gates straddle thin silicon fin**
- **Current flows parallel to wafer surface**



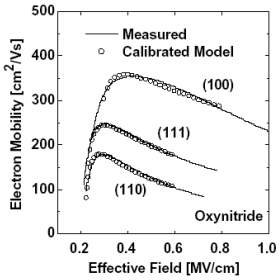
Impact of FinFET Orientation

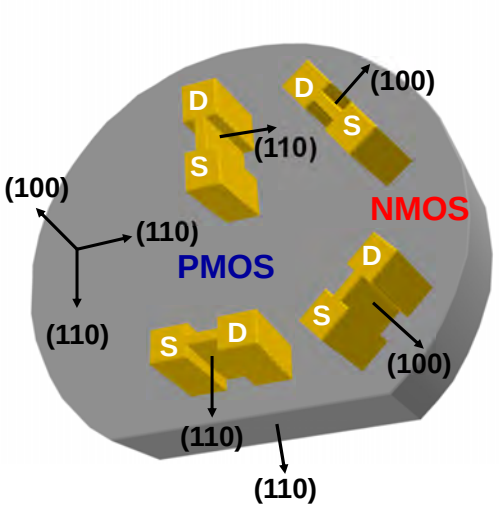
L. Chang *et al.*, *IEEE Trans. Electron Devices*, Vol. 51, p. 1621, 2004

Hole Mobility



Electron Mobility

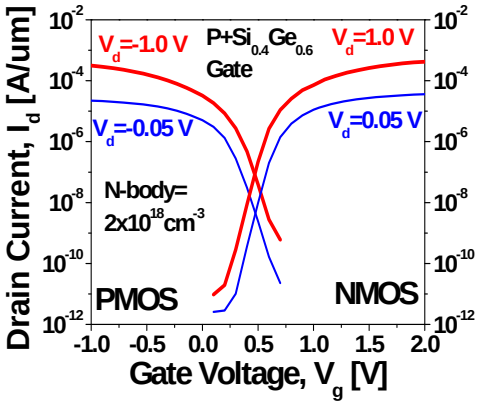




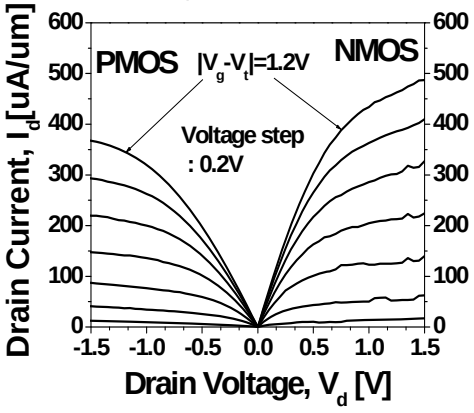
15 nm L_g FinFETs

T_{Si} = 10 nm; T_{ox} = 2.1 nm

Sub-Threshold Characteristics

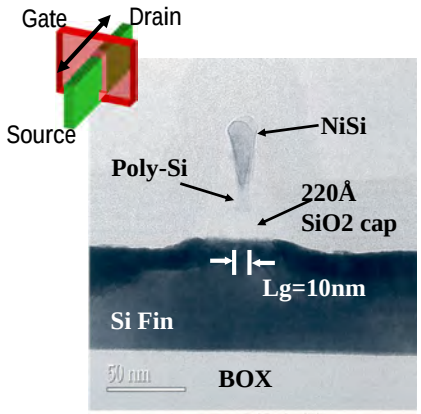


Output Characteristics



Y.-K. Choi *et al.*, *IEDM Technical Digest*, pp. 421-424, 2001

10 nm L_g FinFETs



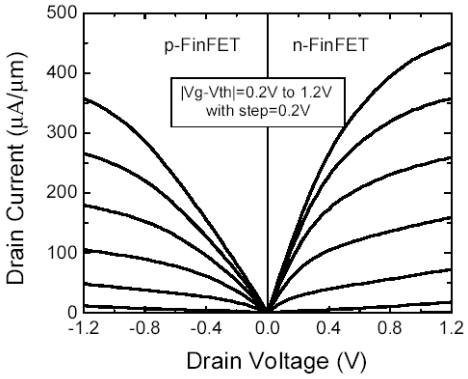
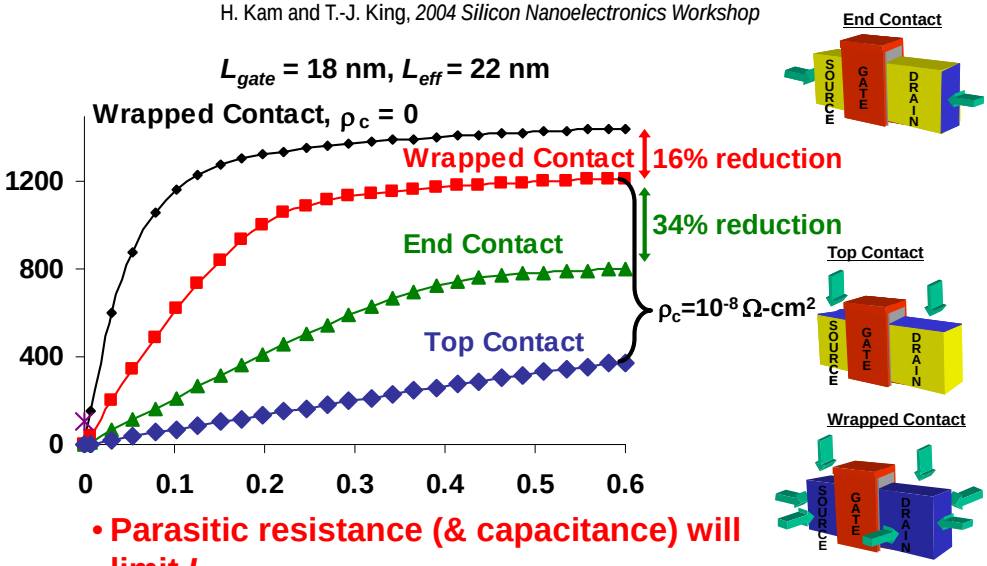


Fig.5 Id-Vd characteristics of 10nm gate length CMOS FinFET transistors.

B. Yu *et al.*, *IEDM Technical Digest*, pp. 251-254, 2002

Impact of S/D Contact Structure

H. Kam and T.-J. King, *2004 Silicon Nanoelectronics Workshop*



- **Parasitic resistance (& capacitance) will limit I_{dsat}**

Dynamic Voltage Scaling

Energy ∝ Dynamic power + Static power

$$E = \alpha C_{EFF} V_{DD}^2 + V_{DD} I_0 e^{-(V_{TH}/S)} T_{CYCLE}$$

Dynamic supply-voltage (V_{DD}) scaling:

- **Reduces dynamic power, but at performance cost**
- **Only option for DG-FET operation**

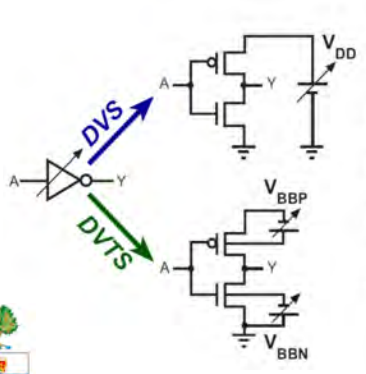
Combined V_{DD} & V_{TH} scaling:

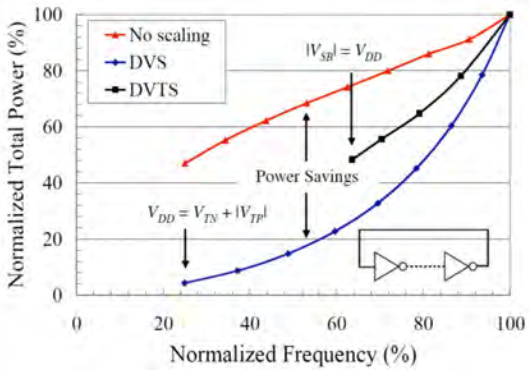
- ✓ **Lowest energy without performance loss**
- **Requires back-gate biasing capability**

Power Management Techniques: DVS & DVTS

- Modern CPUs require aggressive real-time power and thermal management strategies
  - Dynamic Voltage Scaling (DVS)
  - Dynamic Threshold Scaling (DVTS)

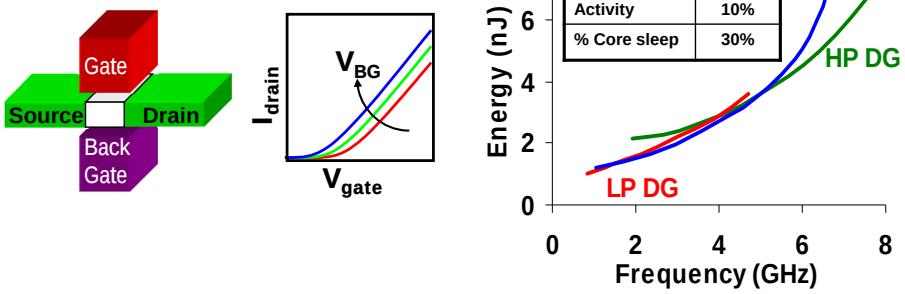
$$P_{dyn} = a \cdot C \cdot V_{DD}^2 \cdot f_{clk}$$





Back-Gated FETs for Dynamic V_T

S. Balasubramanian *et al.*, *2004 SOI Conference*



Back-gated UTB FET spans larger *Energy vs. Delay* space

- 100× lower leakage in sleep mode
  - → energy savings without delay penalty

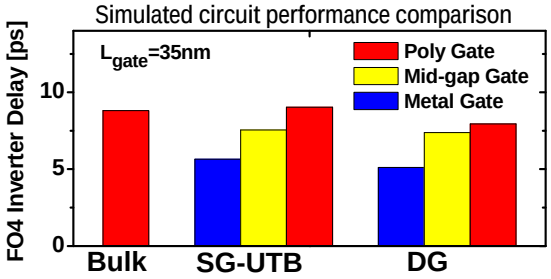
Outline

- Introduction
- Thin-body transistor structures
- Advanced CMOS materials
  - Metal gate technology for thin-body FETs
  - High-κ gate dielectric
- Performance enhancement approaches
- Summary

Impact of Gate Technology

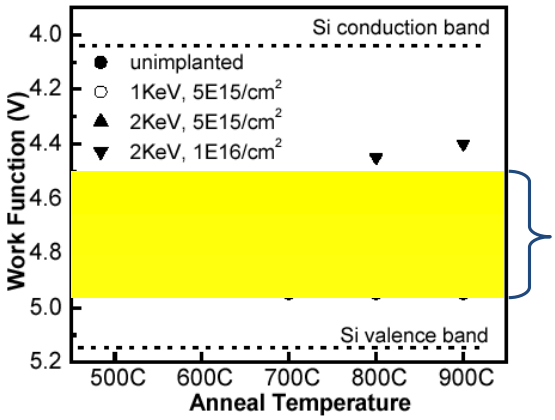
L. Chang *et al.*, *IEDM* 2000

- Channel doping must be eliminated to achieve high I_{dsat} and to avoid V_T variation due to channel dopant fluctuation effects
  - → V_T must be adjusted by tuning the gate work function Φ_M in the range from ~4.5eV to ~5.0eV



Tunable-Φ_M Mo Gate Technology

P. Ranade *et al.*, *IEDM Technical Digest*, pp. 363-366, 2002



- **Effective Φ_M can be selectively lowered by N$^+$ implantation + thermal annealing**

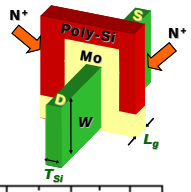
required range

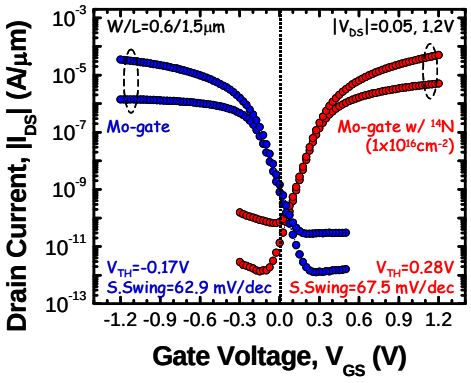
Anneal time = 15m except for 900°C (15s)

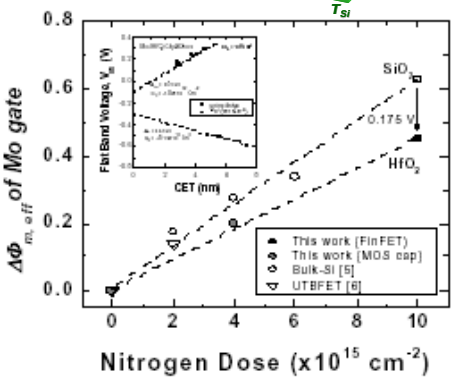
T_{Mo} = 15nm

Mo-gated HfO_2 FinFETs

D. Ha *et al.*, to be presented at *IEDM* 2004



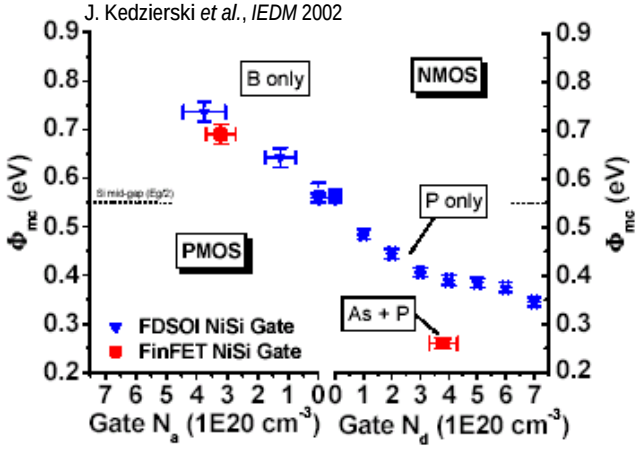




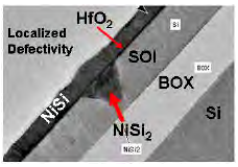
- FinFET gate current is reduced by >10^3, as compared to poly-Si/SiO_2 with same EOT
- Φ_M is reduced by N implantation
  Reduction is lower than on SiO_2, due to N diffusion into the HfO_2

Tunable-Φ_M NiSi Gate Technology

J. Kedzierski *et al.*, *IEDM* 2002



- **Φ_M can be adjusted by implanting Si with dopants prior to Ni silicidation:**
  4.5 eV < Φ_M < 4.9 eV
  (n+ Si) (p+ Si)
- **Potential issues:**
  - dopant penetration
  - thermal stability
  - stress/adhesion
  - gate-oxide reliability



J. Schaeffer *et al.*, *2004 MRS Spring Meeting*
(NiSi gate annealed 60s at 700°C)

Outline

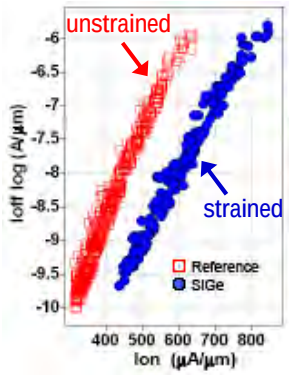
- Introduction
- Thin-body transistor structures
- Advanced CMOS materials
- Performance enhancement approaches
  - Mobility enhancement
  - Metallic source/drain structure
  - Negative differential resistance devices
- Summary

Field-Effect Mobility

- **Increased carrier mobility → improved I_{on} / I_{off} tradeoff**

- Mobilities are dependent on:
  - channel surface orientation & current flow direction
  - gate-stack materials & processes
  - channel strain
- Process-induced strain is dependent on:
  - process conditions (thermal exposure)
  - layer thicknesses and transistor lateral dimensions
    - ⇨ gate length, channel width, S/D length

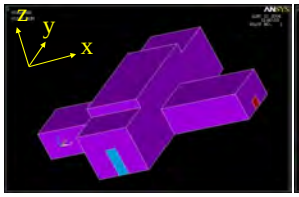
Bulk-Si PMOSFET I_{on} vs. I_{off}



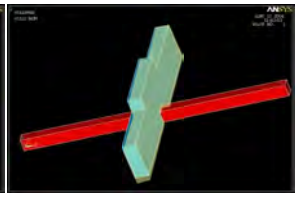
P.R. Chidambaram *et al.*, *Symp. VLSI Technology Digest*, pp. 48-49, 2004

Strained FinFET Approaches

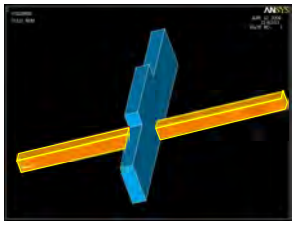
Stressed Capping Layer



Stressed Gate Electrode

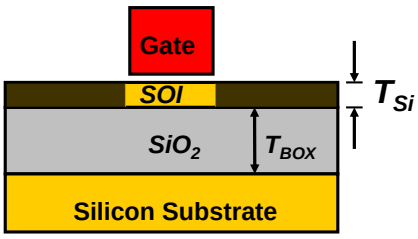


Stressed S/D



Minimizing Parasitic Resistance

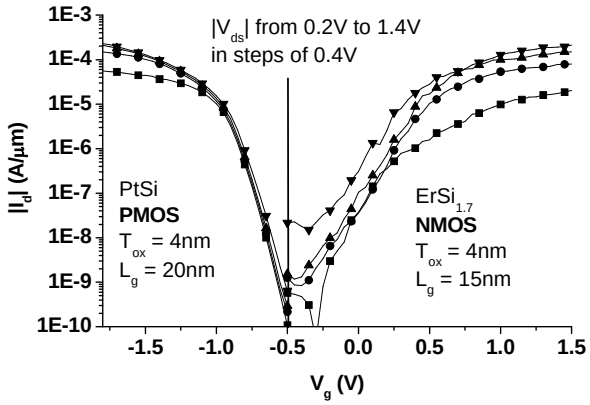
- Need thin-body structure to control leakage
- Use metallic source/drain to minimize R_{series}
  - *e.g.* fully silicided source/drain regions
  - Ideally, Schottky barrier height $\Phi_b \leq 0.1$ eV



- **Advantages:**
  - **improved circuit speed**
  - **simpler process flow**
  - **reduced S/D variations**
  - **enhanced thermal conductivity**

Thin-Body Metallic-S/D MOSFETs

J. Kedzierski *et al.*, *IEDM Technical Digest*, pp. 57-60, 2000



- $T_{Si} \approx$ **10nm**
- PtSi (Φ_{bop}=0.24V) for PMOS S/D
  $ErSi_{1.7}$ (Φ_{bon}=0.28V) for NMOS S/D
- ✓ Excellent I_{off}
- ✓ High NMOS contact resistance due to oxidation of $ErSi_{1.7}$

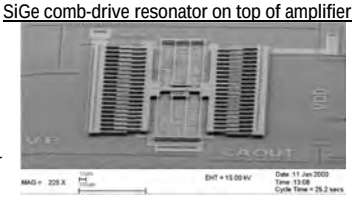
Off the Roadmap…

- Alternative approaches to
  - enhance performance and/or functionality
  - lower power consumption per function

  will be needed to reduce cost per function

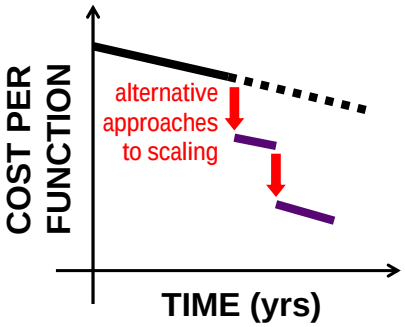
  - ➢ innovative circuit & system design
  - ➢ 3D & heterogeneous integration

SiGe comb-drive resonator on top of amplifier



A. E. Franke *et al.*, *2000 Solid-State Sensor and Actuator Workshop*

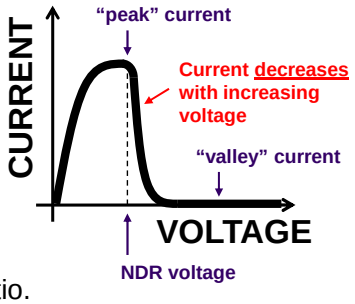
  - ➢ **new devices**



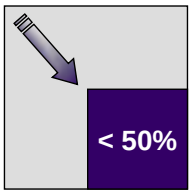
Negative Differential Resistance

- **NDR devices enable more efficient design**

  →lower power & cost, provided that the NDR devices
  - are compact (as small as a FET),
  - are easily integrated with CMOS, and
  - have high "peak" to "valley" current ratio.



layout area comparison



DEVICE COUNT COMPARISON

Circuit	CMOS	NDR + NFET
XOR	16	4
NOR+flip-flop	12	4
SRAM	6	3

P. Mazumder *et al*., *Proc. IEEE* **86**, 664 (1998)

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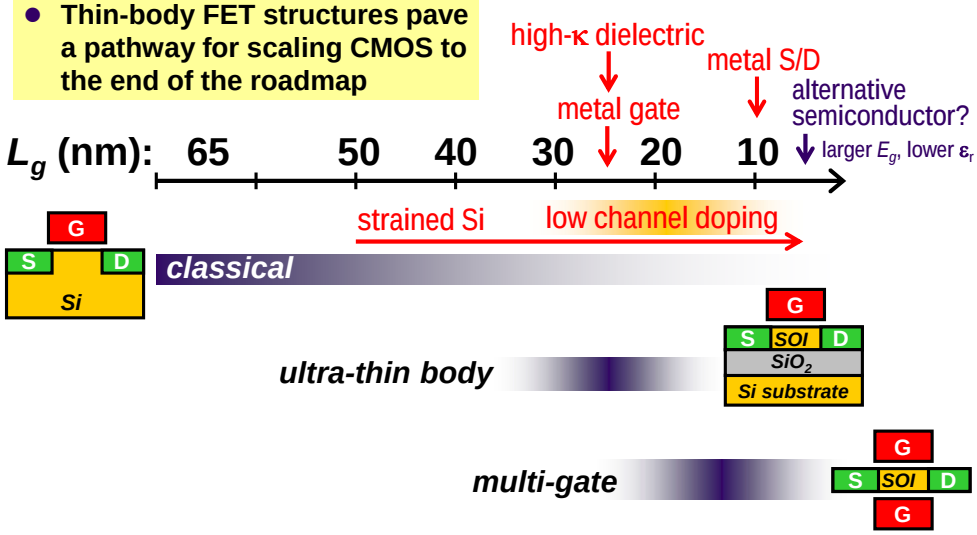
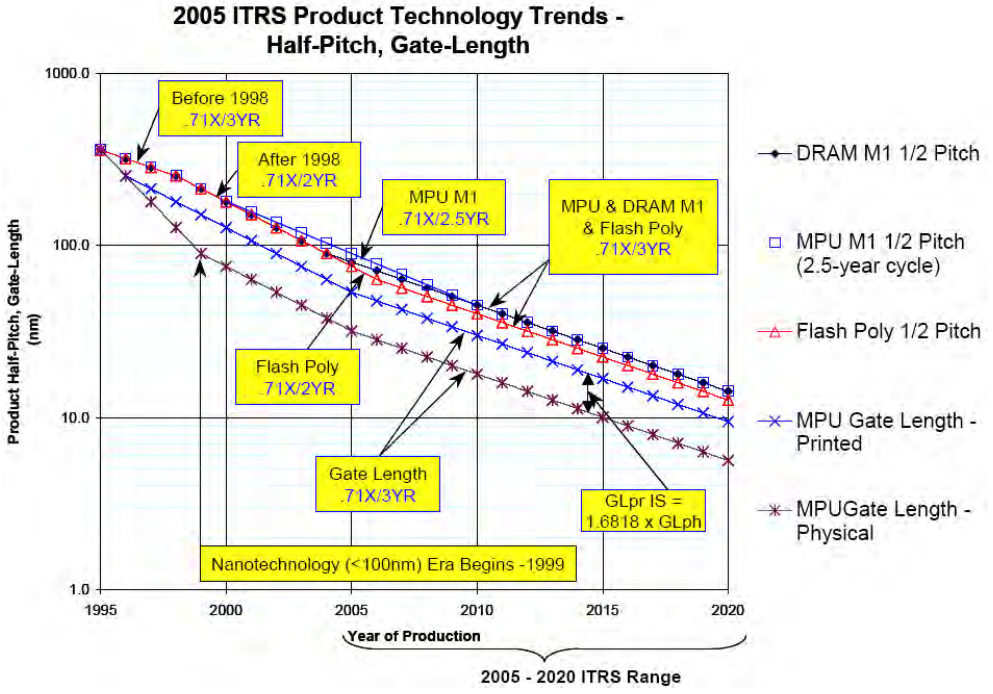
MOSFET Scaling Scenario

- **Thin-body FET structures pave a pathway for scaling CMOS to the end of the roadmap**





ITRS 2015 Summary

- Physical Properties of Transistors

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	FinFET FDSOI	FinFET FDSOI	FinFET LGAA	FinFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm)[1,2]	28.0	18.0	12.0	10.0	6.0	6.0	6.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
Contacted poly half pitch (nm)	35.0	24.0	21.0	16.0	12.0	12.0	12.0
L_g: Physical Gate Length for HP Logic (nm) [3]	24	18	14	10	10	10	10
L_g: Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12

FDSOI fully depleted silicon on insulator
LGAA/VGAA lateral/vertical gate-all-around
M3D materials for a magnetic memory in three dimensions

ITRS 2015 Summary

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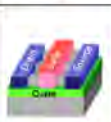
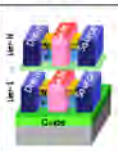
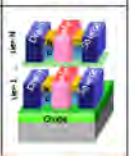
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	FinFET FDSOI	FinFET FDSOI	FinFET LGAA	FinFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
FinFET Fin Half-pitch (new) =0.75 or 1.0 M0/M1 (nm)	21.0	18.0	12.0				
FinFET Fin Width (nm)	8.0	6.0	6.0				
FinFET Fin Height (nm)	42.0	42.0	42.0		END OF	2D	DOMAIN
Footprint drive efficiency - FinFET	2.19	2.50	3.75				
Lateral GAA Lateral Half-pitch (nm)			12.0	10.0			
Lateral GAA Vertical Half-pitch (nm)			12.0	9.0			
Lateral GAA Diameter (nm)			6.0	6.0			
Footprint drive efficiency - lateral GAA, 3x NWs stacked			2.4	2.8	START	OF 3D	DOMAIN

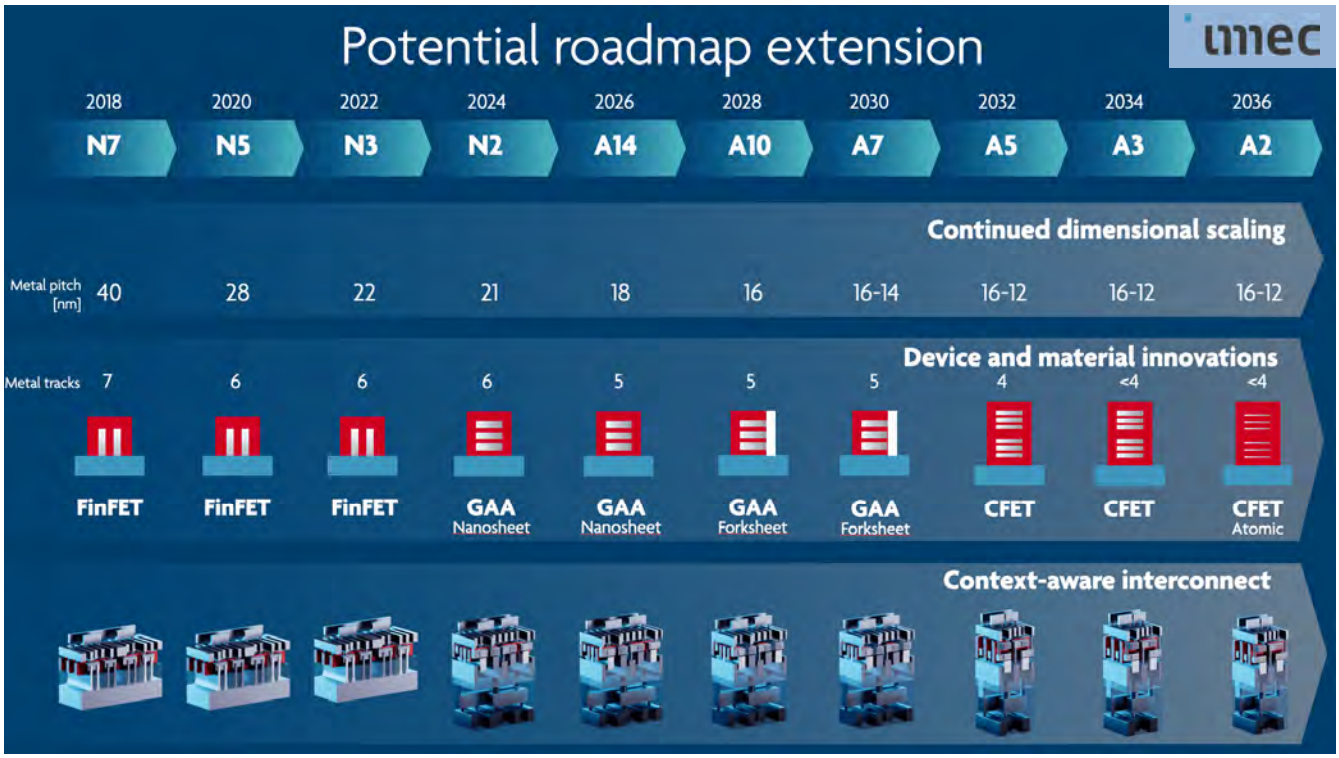
ITRS 2015 Summary

- Physical Properties of Transistors

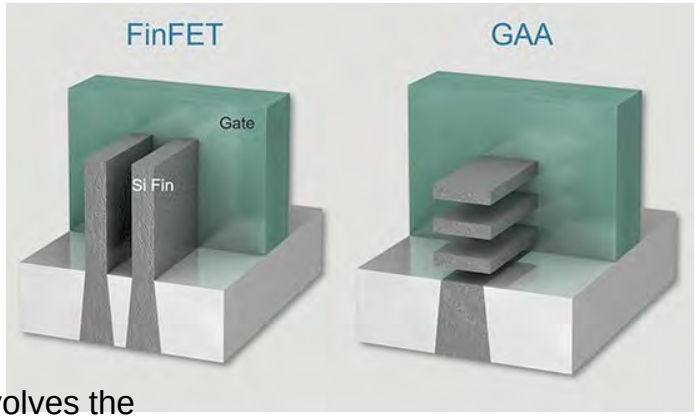
YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	FinFET FDSOI	FinFET FDSOI	FinFET LGAA	FinFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
Vertical GAA Lateral Half-pitch (nm)				10.0	6.0	6.0	6.0
Vertical GAA Diameter (nm)				6.0	5.0	5.0	5.0
Footprint drive efficiency - vertical GAA, 3x NWs stacked				2.8	3.9	3.9	3.9
Device effective width - [nm]	92.0	90.0	56.5	56.5	56.5	56.5	56.5
Device lateral half pitch (nm)	21.0	18.0	12.0	10.0	6.0	6.0	6.0
Device width or diameter (nm)	8.0	6.0	6.0	6.0	5.0	5.0	5.0

To emphasize the transition to 3D Power Scaling the columns describing 2D transistor dimensions have been left FinFET cells completely blank from 2021 on.

YEAR OF PRODUCTION	Edition	2023	2025	2028	2031	2034	2037
	New	2022-FF+	2025-LGAA	2028-LGAA	2031-CFET	2034-CFET	2037-CFET
	Updated	G48M24	G45M20	G42M16	G40M16	G38M16/T2	G38M14/T4
Logic industry "Node Range" Labeling	Updated	"3nm+"	"2nm"	"1.5nm"	"18am eq"	"7am eq"	"5am eq"
Fine-pitch 3D integration scheme	Updated	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	Updated	finFET LGAA	LGAA	LGAA	LGAA-3D CFET	LGAA-3D CFET	LGAA-3D CFET
Backside structure options	New	-	Backside via	Direct contact	Decap+ESD	Active devices	Active devices
Platform device for logic	Updated	finFET	LGAA	LGAA	CFET	CFET	CFET
	Updated						
LOGIC DEVICE GROUND RULES							
Mx pitch (nm)	Updated	32	24	20	16	16	14
M1 pitch (nm)	Updated	32	23	21	20	19	19
M0 pitch (nm)	Updated	24	20	16	16	16	14
Gate pitch (nm)		48	45	42	40	38	38
Lg: Gate Length - HP (nm)		16	14	12	12	12	12
Lg: Gate Length - HD (nm)		18	14	12	12	12	12
Channel overlap ratio - two-sided		0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)		6	6	5	5	4	4
Spacer k value		3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA		20	19	20	18	18	18
Device architecture key ground rules							
Device lateral pitch (nm)		24	26	24	24	22	22
Device height (nm)		48	52	67	80	75	70
FinFET Fin width (nm)		5.0					
Footprint drive efficiency - finFET		4.21					
Lateral GAA vertical pitch (nm)			18.0	17.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)			6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device	Updated		3	4	5	5	5
LGAA width (nm) - HP	Updated		30	20	15	15	15
LGAA width (nm) - HD			15	10	10	6	6
LGAA width (nm) - SRAM			7	6	6	6	6
Footprint drive efficiency - lateral GAA - HP			4.41	5.47	6.36	6.45	6.13
Device effective width (nm) - HP		101.0	216.0	208.0	210.0	200.0	190.0
Device effective width (nm) - HD		101.0	126.0	128.0	160.0	110.0	100.0
PN seperation width (nm)	Updated	45	40	30			
PN seperation vertical space (nm)	New				20	20	20



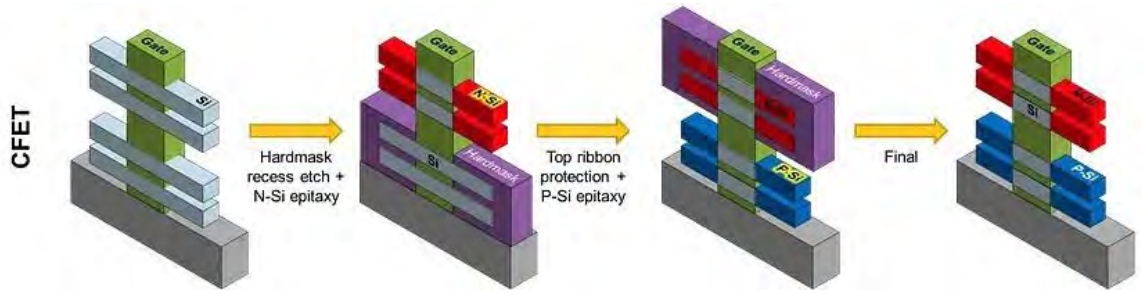
FinFETs and CFETs



- When transistor sizes shrink to below 30 nm, the short-channel effects become prominent
- FinFET - a 3D transistor structure where the gate surrounds a thin fin-shaped channel
- GAAFET - Further innovation involves the gate completely surrounding the channel, not limited to the bottom and sides
- Nanosheet is a variant of GAAFET, where the transistor's channel consists of multiple thin-sheet materials, and the gate surrounds these sheets

FinFETs and CFETs

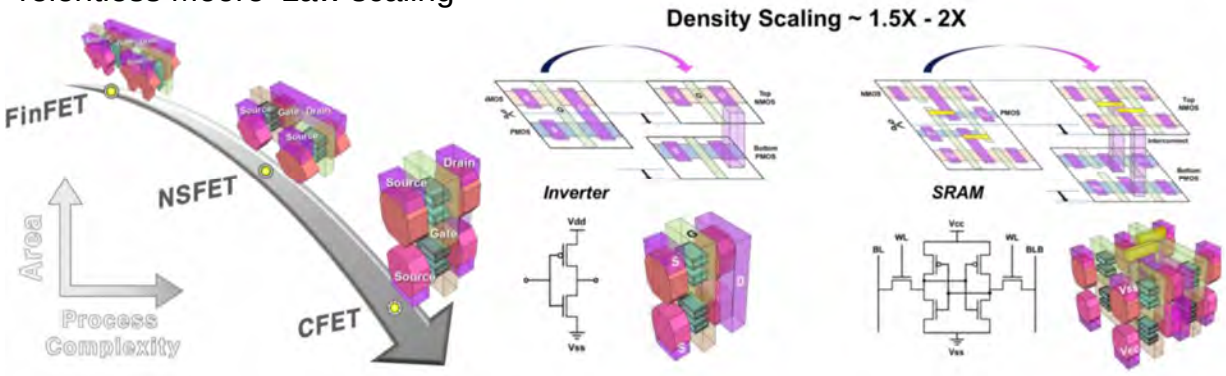
- CFET - a p-type Nanosheet FET is vertically stacked on top of an n-type Nanosheet FET, forming a three-dimensional transistor



https://www.tech-sparks.com/cfet-transistor/?form=MG0AV3

Evolution of the FinFET

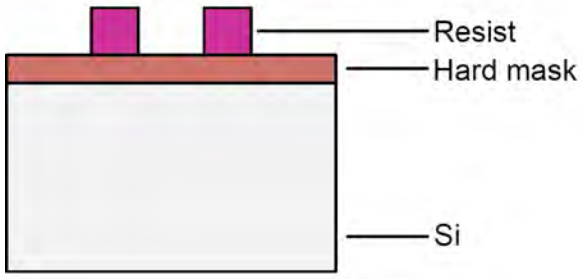
- Device architectures evolve from the FinFET, include the Nanosheet FET (NSFET), 3-D stacked CFET architecture.
- Novel transistor architecture innovations keep fueling the energy to drive relentless Moore' Law scaling



S. Liao *et al*., "Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling," *2023 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2023, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413672

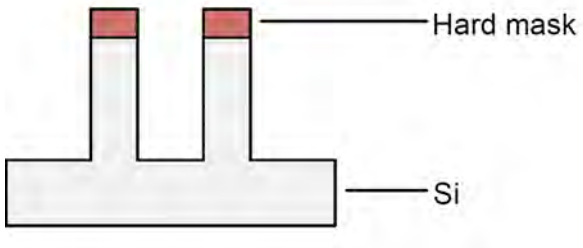
Construction of a bulk silicon-based FinFET

- **Substrate**: Basis for a FinFET is a lightly p-doped substrate with a hard mask on top (e.g., silicon nitride) as well as a patterned resist layer.



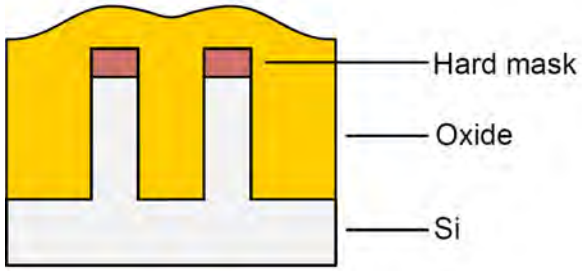
Construction of a bulk silicon-based FinFET

- **Fin etch**: The fins are formed in a highly anisotropic etch process. Since there is no stop layer on a bulk wafer as it is in SOI, the etch process has to be time based. In a 22 nm process the width of the fins might be 10 to 15 nm, the height would ideally be twice that or more.



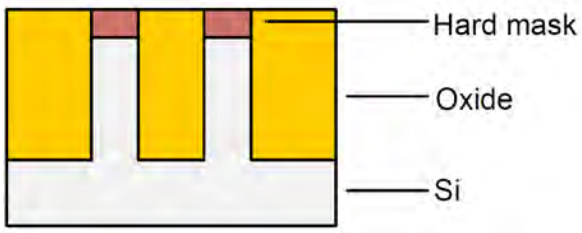
Construction of a bulk silicon-based FinFET

- **Oxide deposition**: To isolate the fins from each other, an oxide deposition with a high aspect ratio filling behavior is needed.



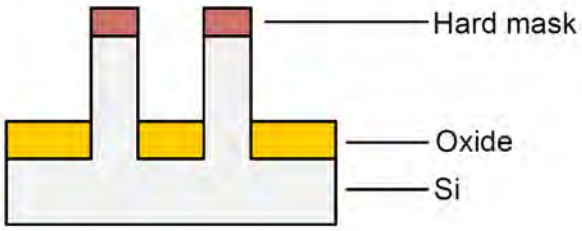
Construction of a bulk silicon-based FinFET

- **Planarization**: The oxide is planarized by chemical mechanical polishing. The hard mask acts as a stop layer.



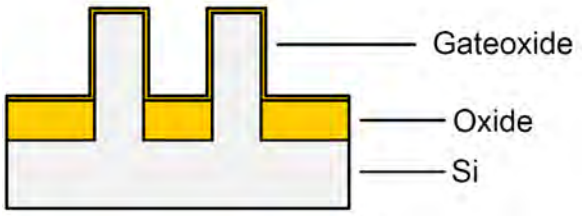
Construction of a bulk silicon-based FinFET

- **Recess etch:** Another etch process is needed to recess the oxide film to form a lateral isolation of the fins.



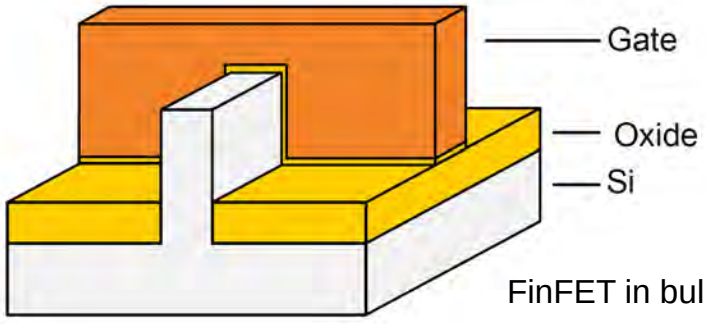
Construction of a bulk silicon-based FinFET

- **Gate oxide:** On top of the fins the gate oxide is deposited via thermal oxidation to isolate the channel from the gate electrode. The fins are still connected underneath the oxide, a high-dose angled implant at the base of the fin creates a dopant junction and completes the isolation (not illustrated).



Construction of a bulk silicon-based FinFET

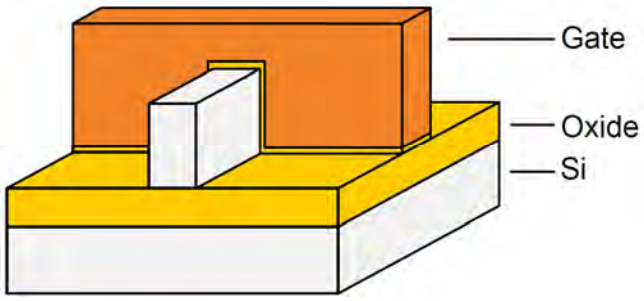
- **Deposition of the gate**: Finally, a highly n+-doped poly silicon layer is deposited on top of the fins. Three gates are wrapped around the channel: one on each side of the fin, and - depending on the thickness of the gate oxide on top - a third gate above.



FinFET in bulk process

Construction of a bulk silicon-based FinFET

- **FinFET on SOI**: Since there is a buried oxide (BOX) layer on an SOI wafer, the channels are naturally isolated from each other. In addition, the etch process of the fins is simplified as the process can be stopped on the oxide easily



FinFET on SOI